Freescale Semiconductor
User's Guide

Document Number: KTPF0100UG
Rev. 2.0, 2/2013

KITPF0100EPEVBE Evaluation Board

Featuring the MMPF0100 14-Channel Configurable PMIC

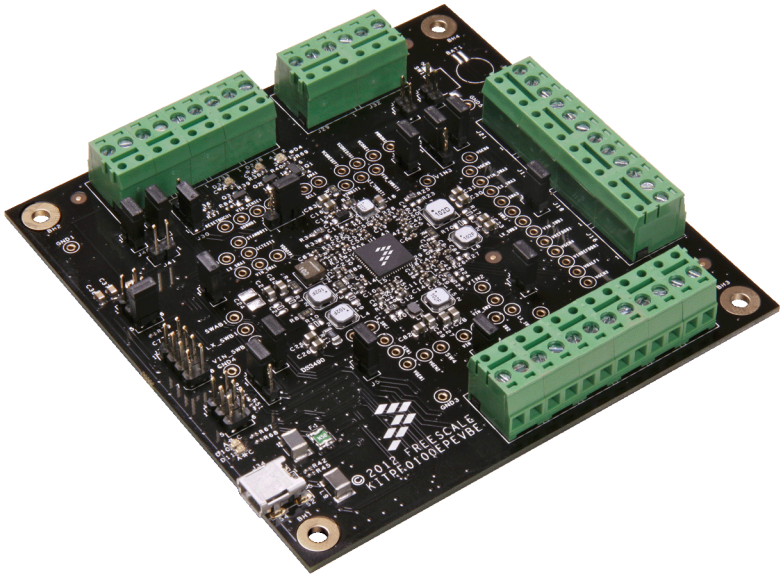


Figure 1. KITPF0100EPEVBE Evaluation Board

Contents

1 Kit Contents / Packing List

- Customer evaluation board KITPF0100EPEVBE
- KITPF0100EPEVBE Quick Start Guide
- Warranty card and Technical support brochure

2 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typical”, must be validated for each customer application by customer’s technical experts.

Freescale does not convey any license under its patent rights nor the rights of others. Freescale products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale product could create a situation where personal injury or death may occur.

Should Buyer purchase or use Freescale products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale was negligent regarding the design or manufacture of the part.Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

3 Introduction

The KITPF0100EPEVBE evaluation board allows full evaluation capability of the PF0100 PMIC for the i.MX6 family of application processors. It provides access to all output voltage rails as well as control and signal pins through terminal block connectors for an easier out-of-the-box evaluation experience. A single terminal block connector for the input power supply allows the user to supply the board with an external DC power supply to fully evaluate the performance of the device.

The KITPF0100EPEVBE comes with a non-programmed version of the PF0100 PMIC, so it is prepared to power up from the default sequence. However, an integrated control/fuse programming interface is provided to allow the customer to program the OTP/TBB (One Time Programmable/Try-Before-Buy) memory and also to select it as the default source for the power-up configuration. Likewise, the programming interface allows full control of the PF0100 through the I^2C communication lines.

This document is intended to provide an overview of the KITPF0100EPEVBE evaluation board as well as detailed instruction for programming the PF0100 through its dedicated Graphic User Interface (GUI).

Note: This document provides updated information on the installation and use of the current PF0100 EVK Control GUI, revision 3.0.0.20. Some discrepancies may be found if using an earlier version of the GUI. To learn about the version of the GUI you are using, please refer to section “Graphical User Interface Description”.

4 KITPF0100EPEVBE Features

- Input voltage operation range from 3.1 V to 4.5 V
- Output voltage supplies accessible through detachable terminal blocks
  - Four to six independent buck converters
  - One 5.0 V boost regulator
  - Six general purpose LDO regulators
  - One DDR memory termination voltage reference
  - One VSRTC supply
- Coin cell support for “Try-Before-Buy” (TBB) mode
- On/off push button support
- Hardware configuration flexibility through various jumper headers and resistors
- Integrated USB to I^2C programming interface for full control/configuration
  - Onboard OTP programming supply and control
  - Onboard PMIC control through the I^2C register map
  - Fully featured programmer through J36 for external device control/programming
- On board connectors for interfacing with future evaluation/debug tools
- Compact form factor (4 x 4 in^2)

5 Hardware/Software Requirements

5.1 Hardware Requirements

- Power supply:
  - Output voltage range from 3.1 V to 4.5 V
  - Current capability from 3 to 5 A (current requirement is dependent on output loading)
- Supply to board connection cables (capable of withstanding up to 5 A current)
- USB (male) to mini USB (male) communication cable.
- USB-enabled computer.

5.2 Software Requirements

- Windows XP or Windows 7 operating system
- Microsoft .NET Framework 4.0
- NI-VISA 5.1.2 communication package + development support with .NET Framework 4.0 languages support
- KITPF0100GUI.zip: Graphical User Interface (GUI) for KITPF0100EPEVBE

6 Software and Drivers Installation

1. Install Microsoft .NET Framework 4.0, download and run "dotNetFx40_client_x86_x84.exe". Click on link below
   http://www.microsoft.com/en-us/download/details.aspx?id=24872
2. Install Windows Installer 3.1 (Windows XP Only), download and run "WindowsInstaller-KB93803-v2-x86.exe".Onl Click on link below
   http://www.microsoft.com/en-us/download/details.aspx?id=25
3. Install NI-VISA 5.1.2, download and run "visa512.exe". Click on link below
   NI-VISA 5.1.2 - National Instruments

Note: It is the customer's responsibility to obtain any license files from National Instruments that are necessary for enabling the NI-VISA 5.1.2 drivers.

When installing the NI-VISA 5.1.2, make sure to select the .NET Framework 4.0 Language Support drivers as shown in Figure 2.

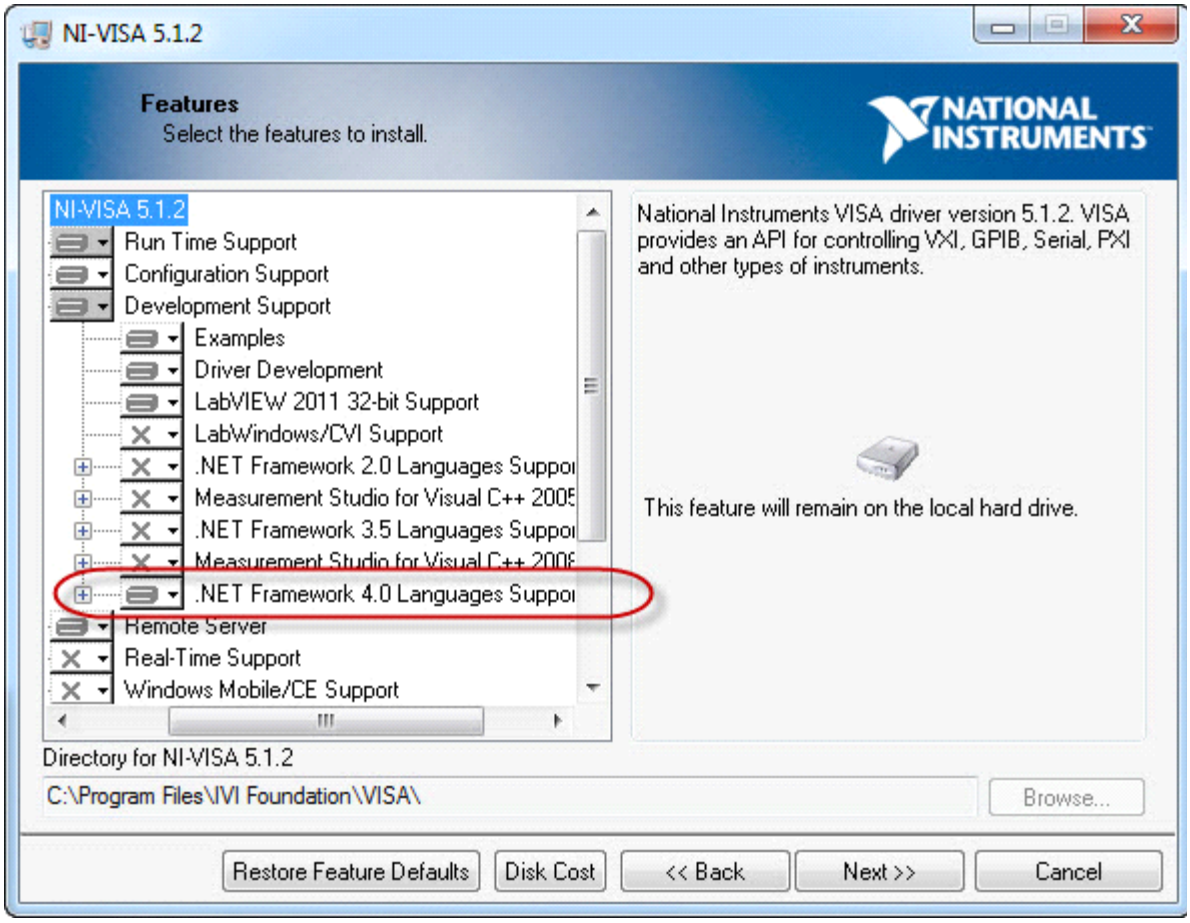


Figure 2. NI-VISA 5.1.2 Features Install window

6.1 Using NI VISA Driver Wizard to install .INF file

1. Go to Start > Programs > National Instruments > VISA > Driver Wizard
2. Select USB under Hardware Bus Selection and press “Next” button

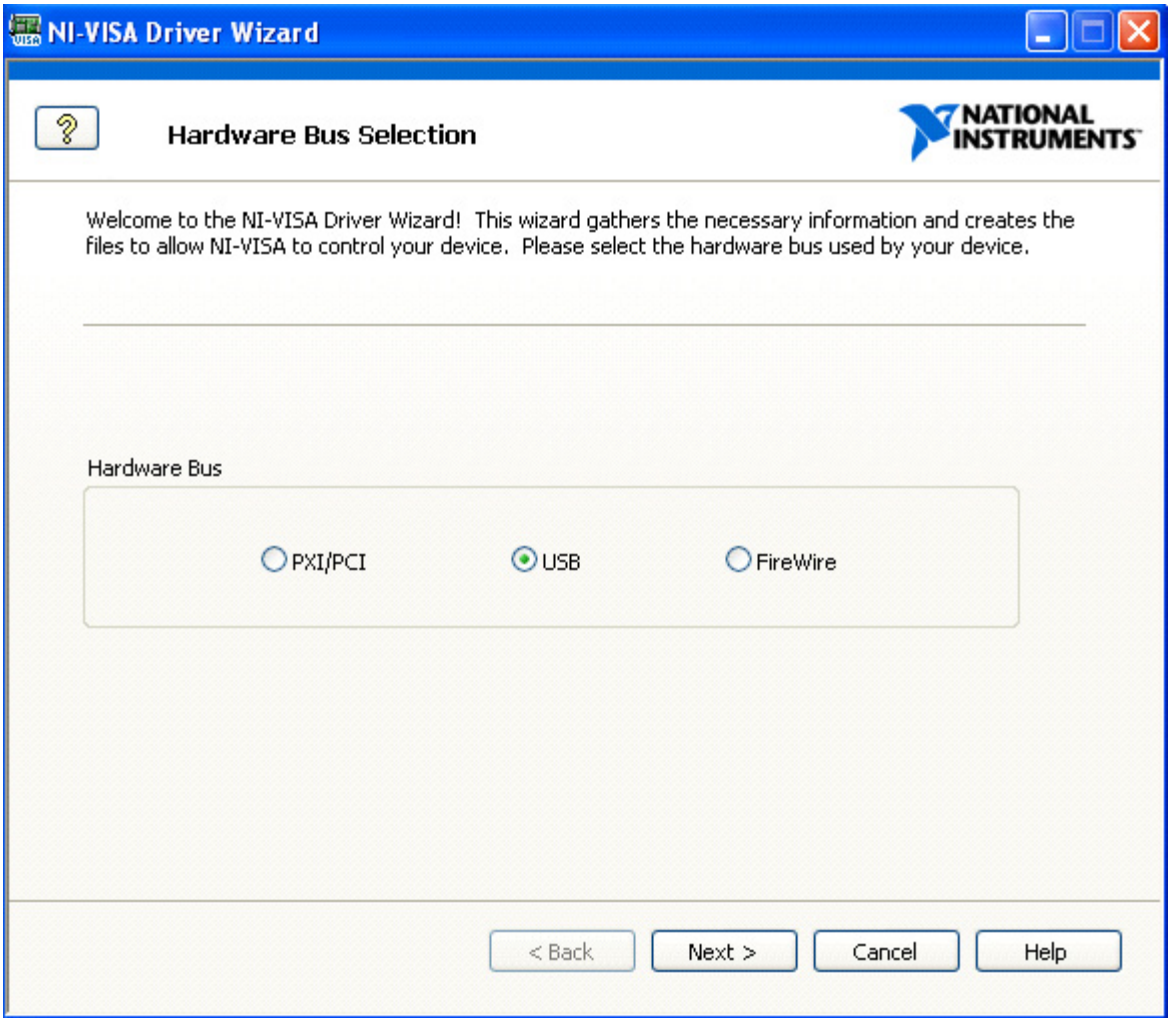


Figure 3. NI-VISA Hardware Bus Selection Window

3. Enter "15A2" in the vendor ID and "00F5" in the product ID fields and press the “Next” button.

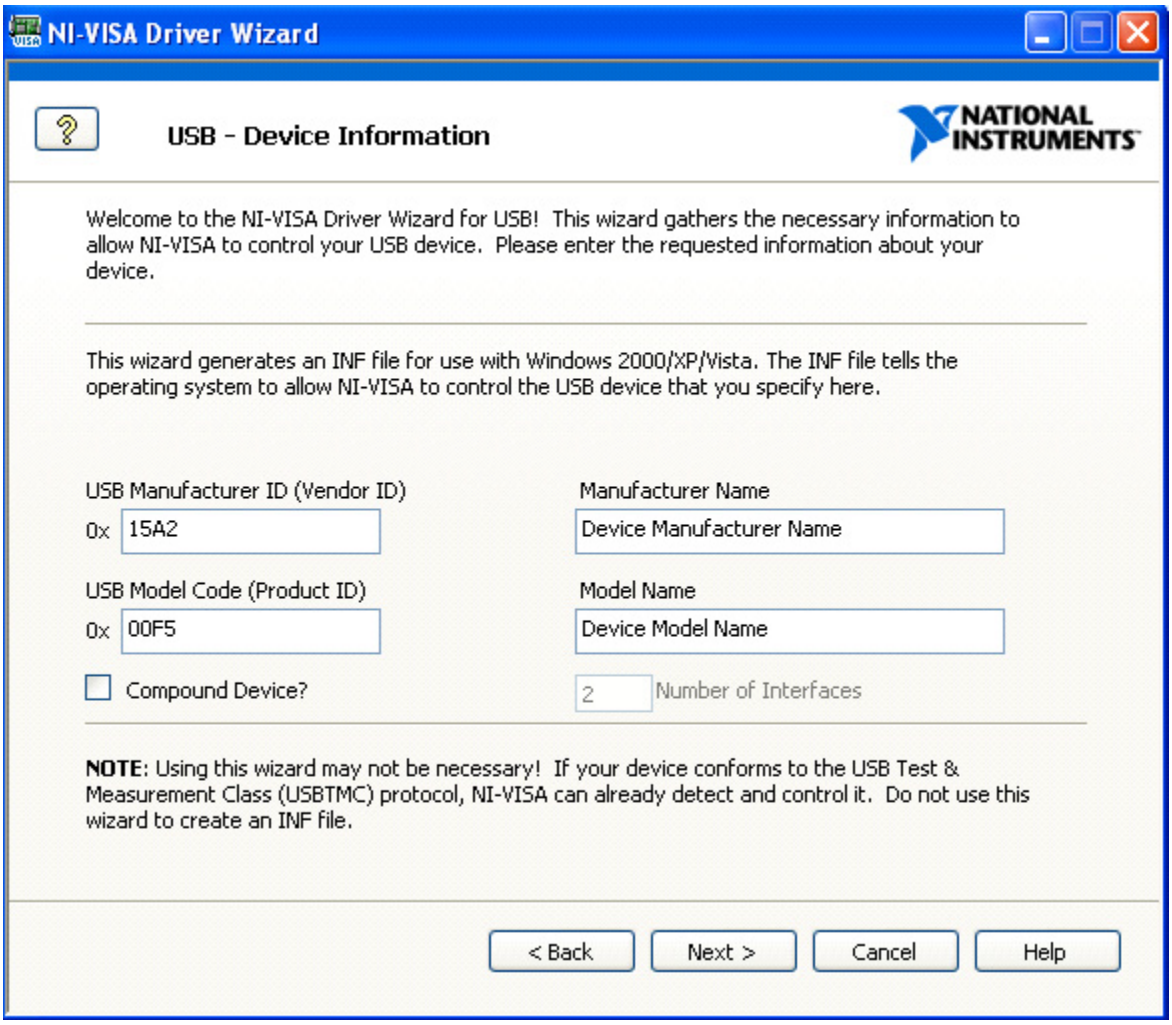


Figure 4. NI-VISA USB Device Information Window

4. Enter "PF0100-Evaluation" in the instrument prefix field, browse to a folder where you want to save the output file and press the “Next” button

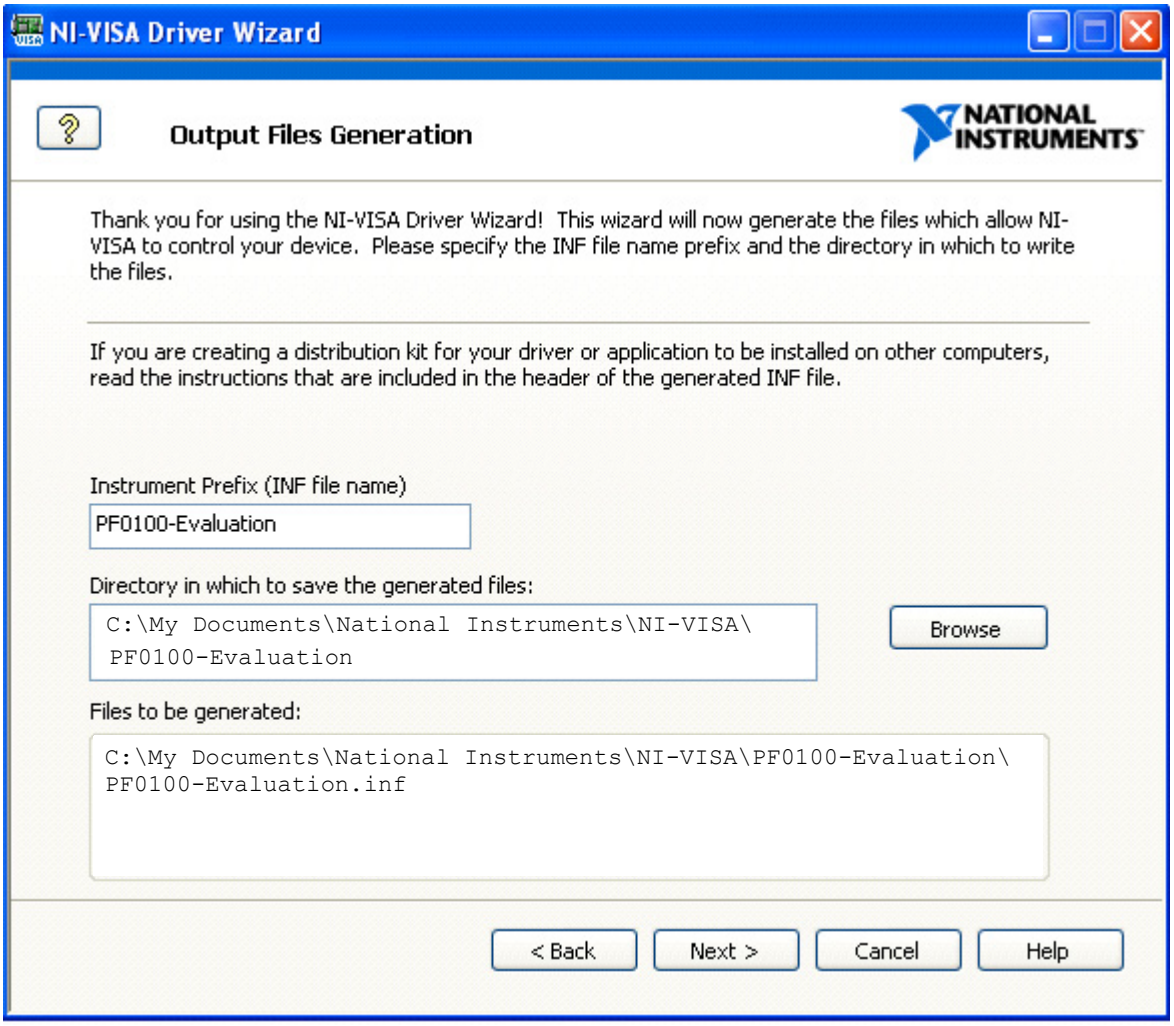


Figure 5. NI-VISA Output File Generation Window

5. Select the option of automatically installing the generated .INF driver and press the “Finish” button.

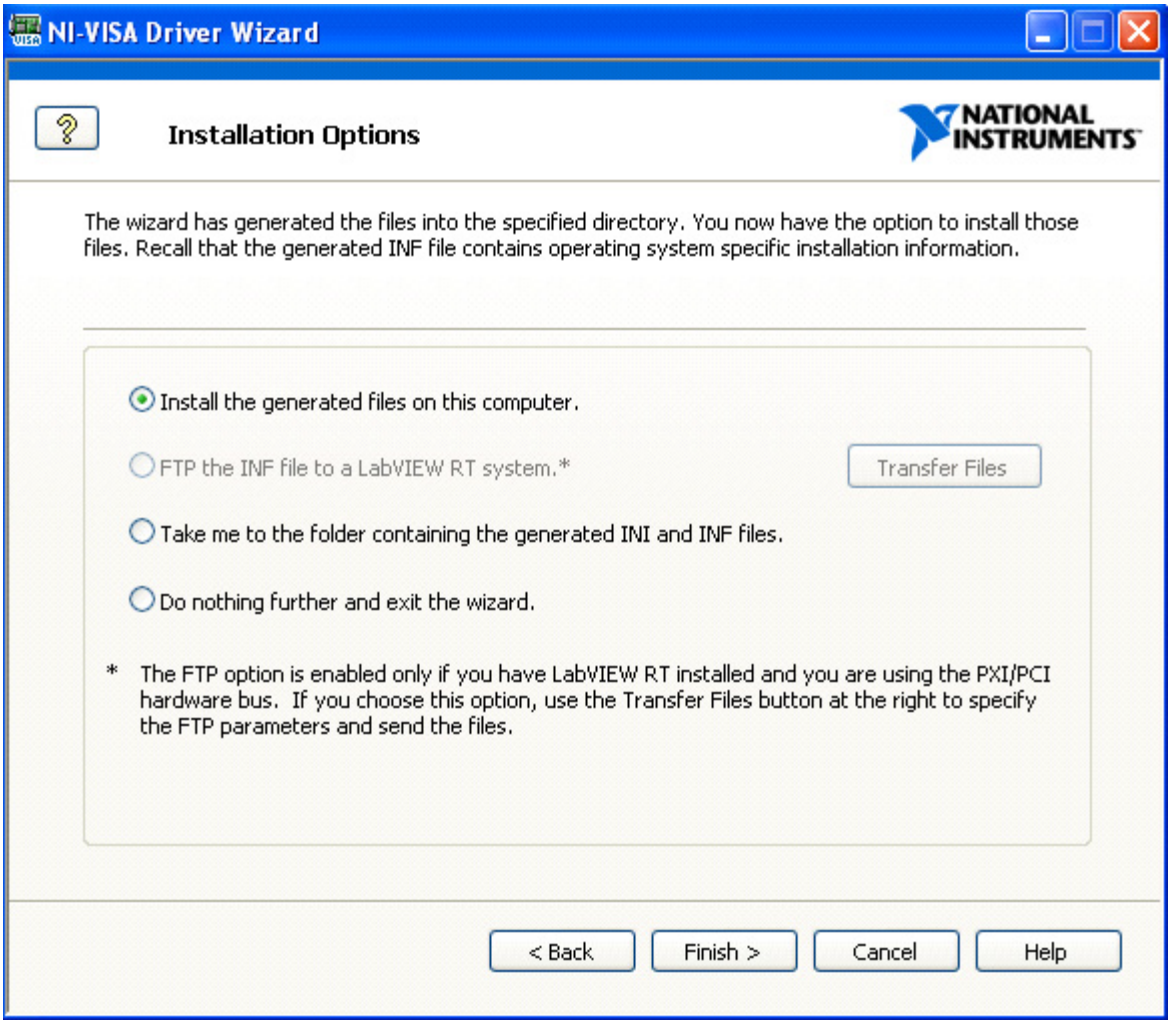


Figure 6. NI-VISA Installation Options Window

6. Supply 3.6V to J25 of KITPFGMEVME and then connect the USB cable from the USB-MiniB port (J34) to the computer. See Figure 10 for the connection diagram.

7. To check if the USB device driver was installed correctly, go to Start > Setting > Control Panels> System > Device Driver. You should see "PF0100-Evaluation Board" under "NI-VISA USB Devices".

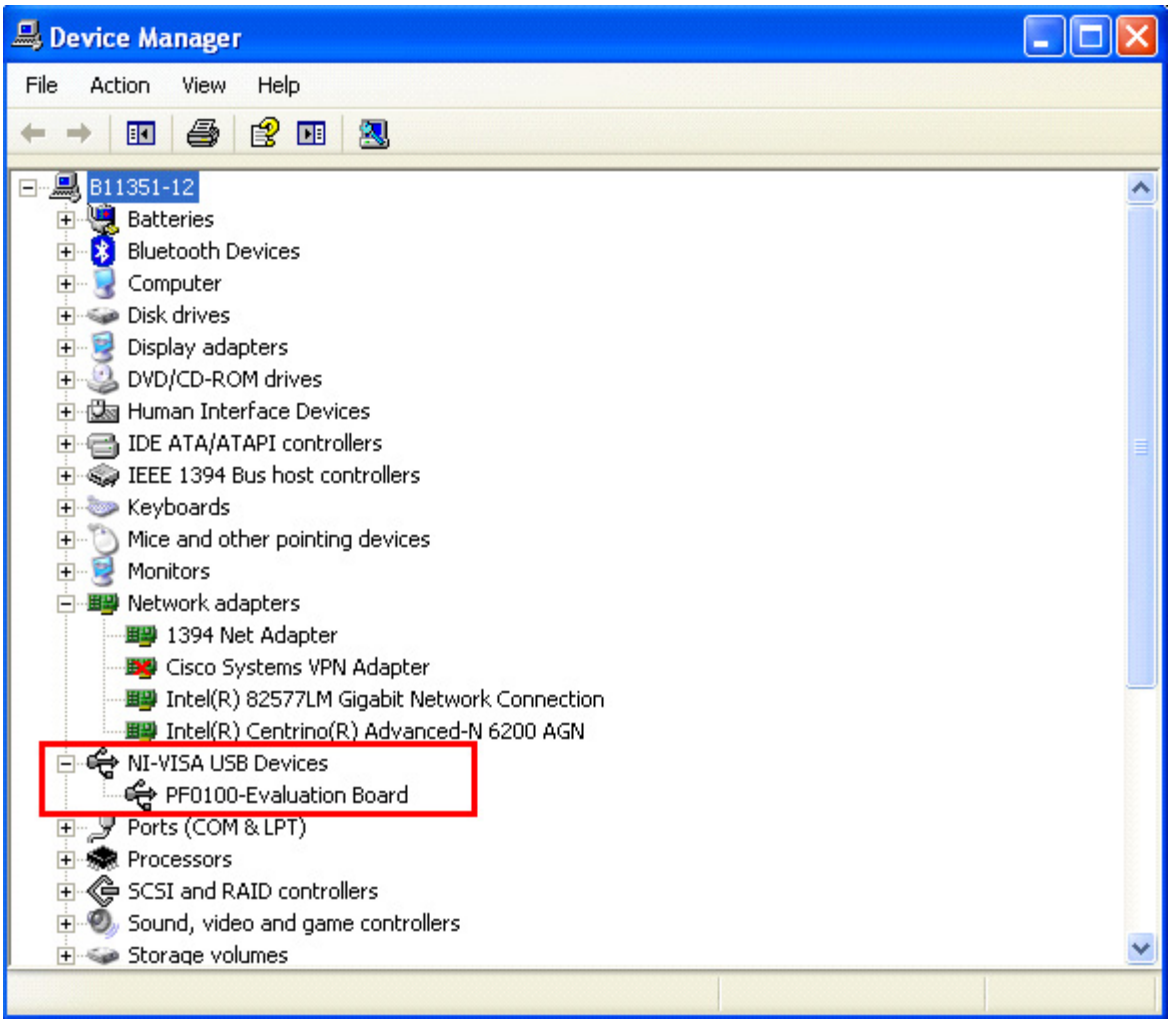


Figure 7. Microsoft Windows Device Manager

6.2 Installing the KITPF0100GUI

1. Create a directory on your PC as follows:
   C:\Freescale\KITPF0100
2. Extract the KITPF0100GUI.zip file into that directory.
3. Launch the "setup.exe" program.
4. When the following popup dialog appears, press the “Install” button.

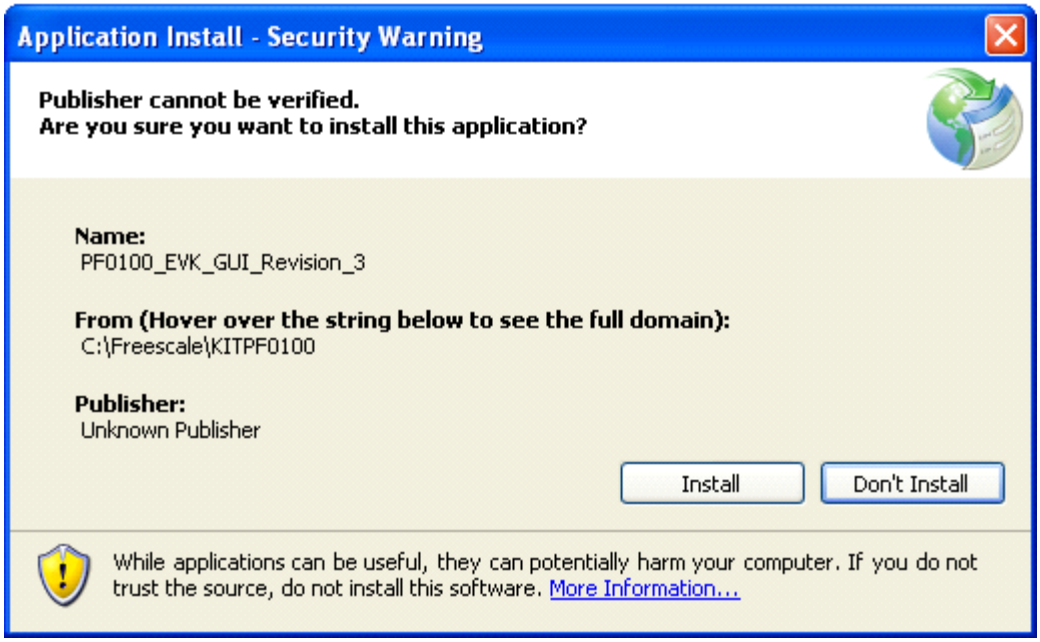


Figure 8. KITPF0100 GUI installation Window

If everything installs correctly, the next screen you should see is the application GUI.

7 Hardware Configuration

By default, the KITPF0100EPEVBE evaluation board is set to power up from the default power-up sequence. Verify that the jumpers are placed in the right position as shown in Figure 9. For a detailed description of the jumper functionality, refer to Table 1.

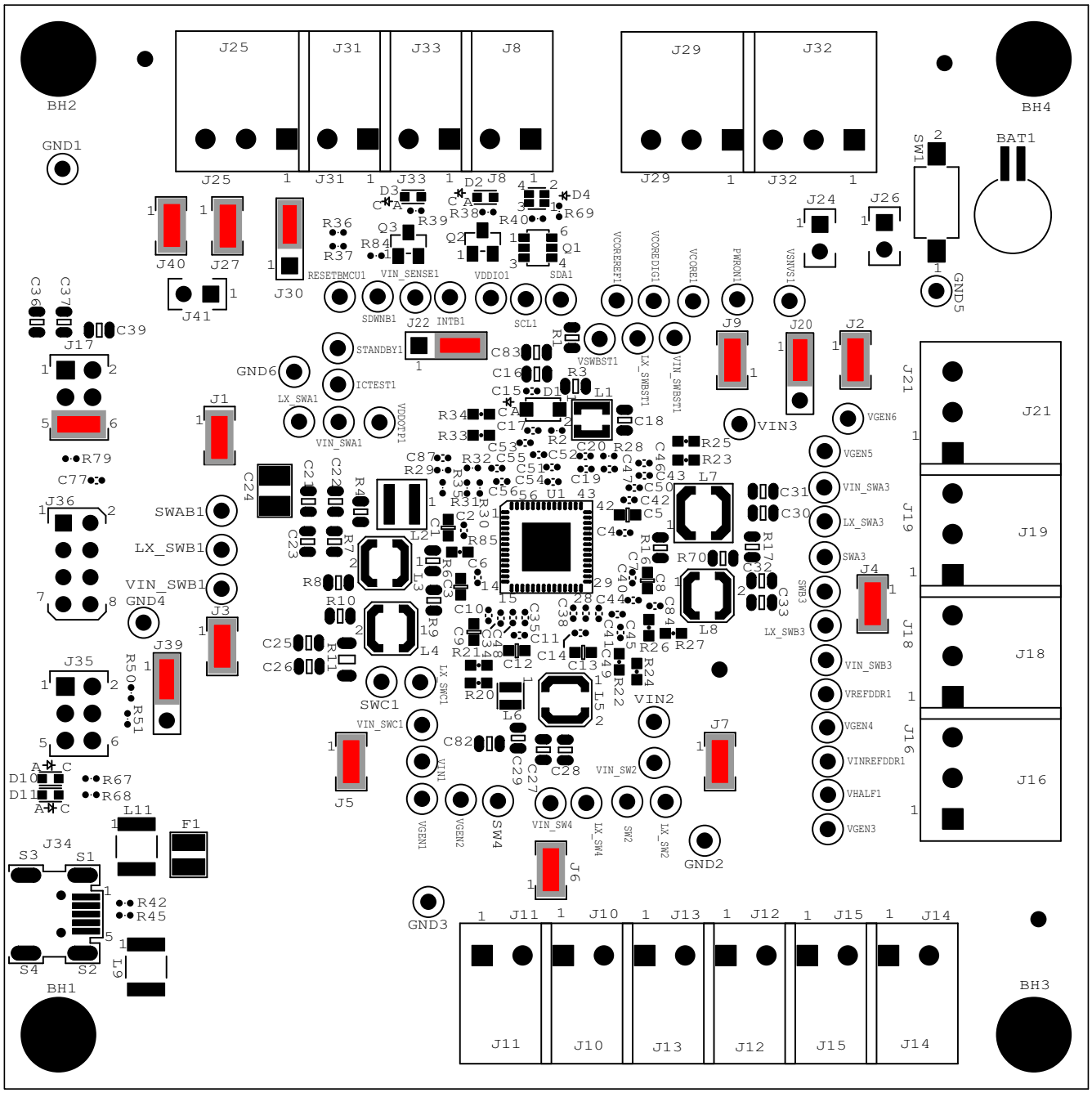


Figure 9. Default Jumper Configuration Diagram

Connect the power supply and the USB communication cables as shown in Figure 10. Voltmeters are optional but it are recommended in order to accurately verify that each one of the output supplies is providing the correct voltage level.

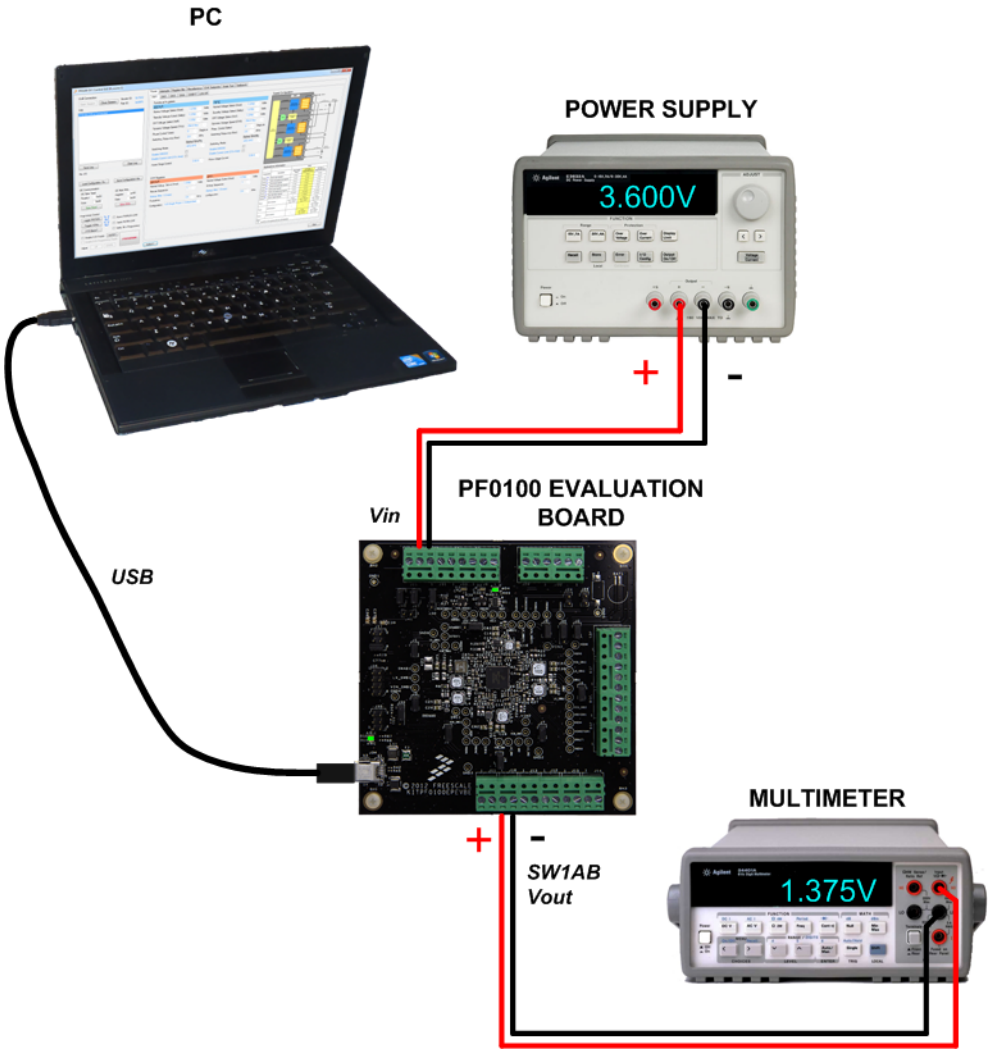


Figure 10. Evaluation Board Setup

Note: The KITPF0100EPEVBE allows the selection of SW2 regulator output or an external 3.3V LDO output as the VDDIO/I^2C pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J30 = 3-2). If the SW2 regulator is to be set below 3.0V then make sure the 3.3V LDO output is connected to VDDIO and the I^2C pull-up resistors by removing R34 and R33 and shorting pins 1, 2 and 3 of J30.

8 Evaluation Board Schematic

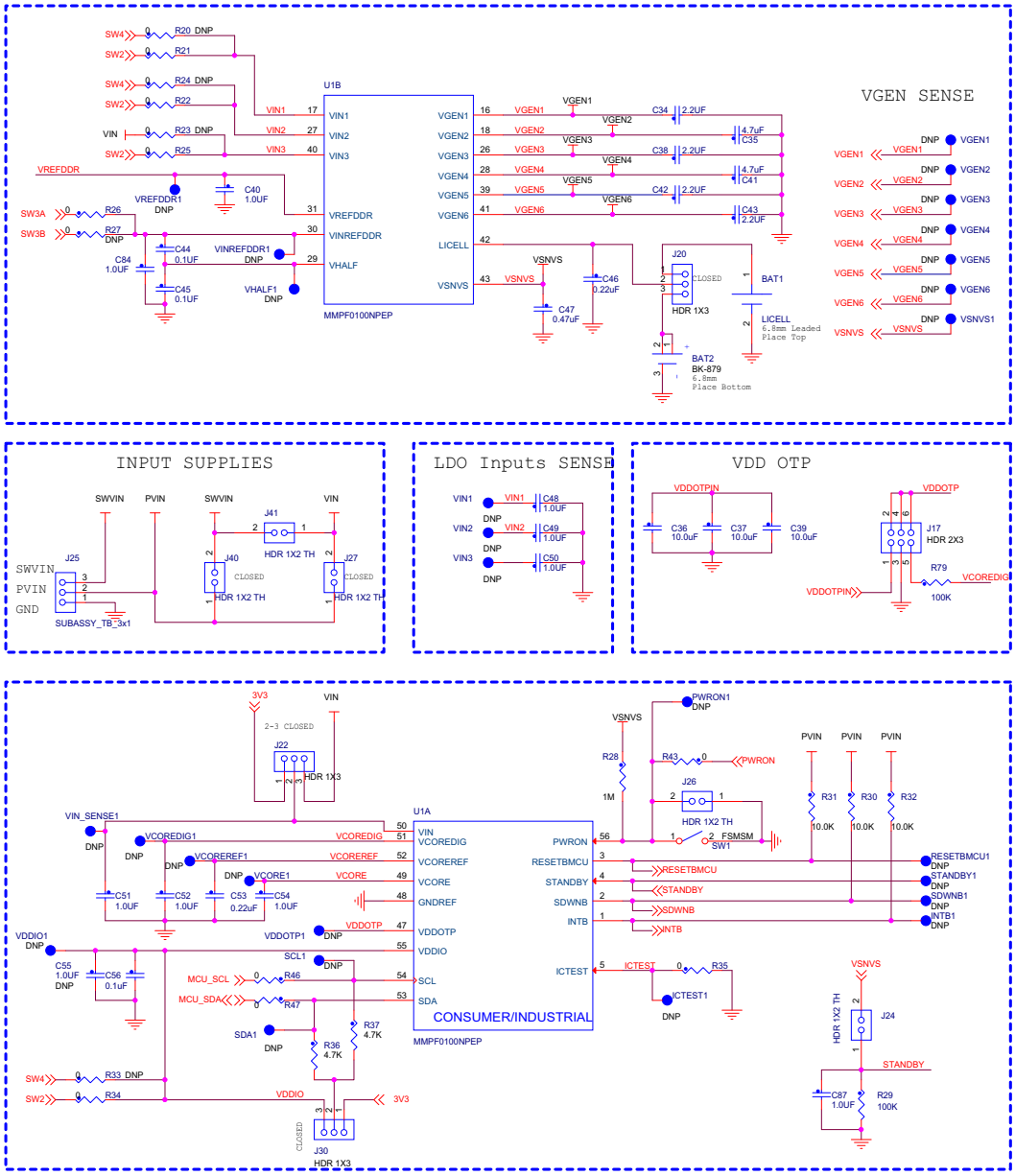


Figure 11. KITPF0100EPEVBE LDO/Control Schematic Part 1

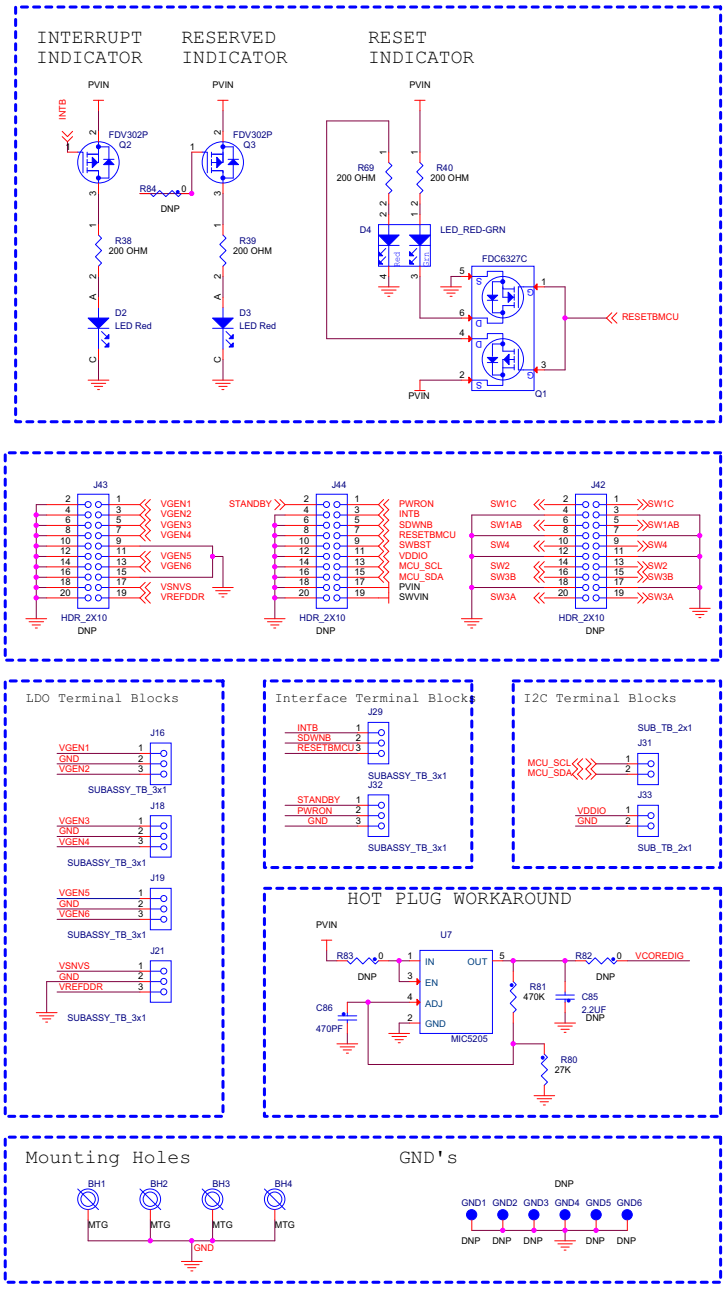


Figure 12. KITPF0100EPEVBE LDO/Control Schematic Part 2

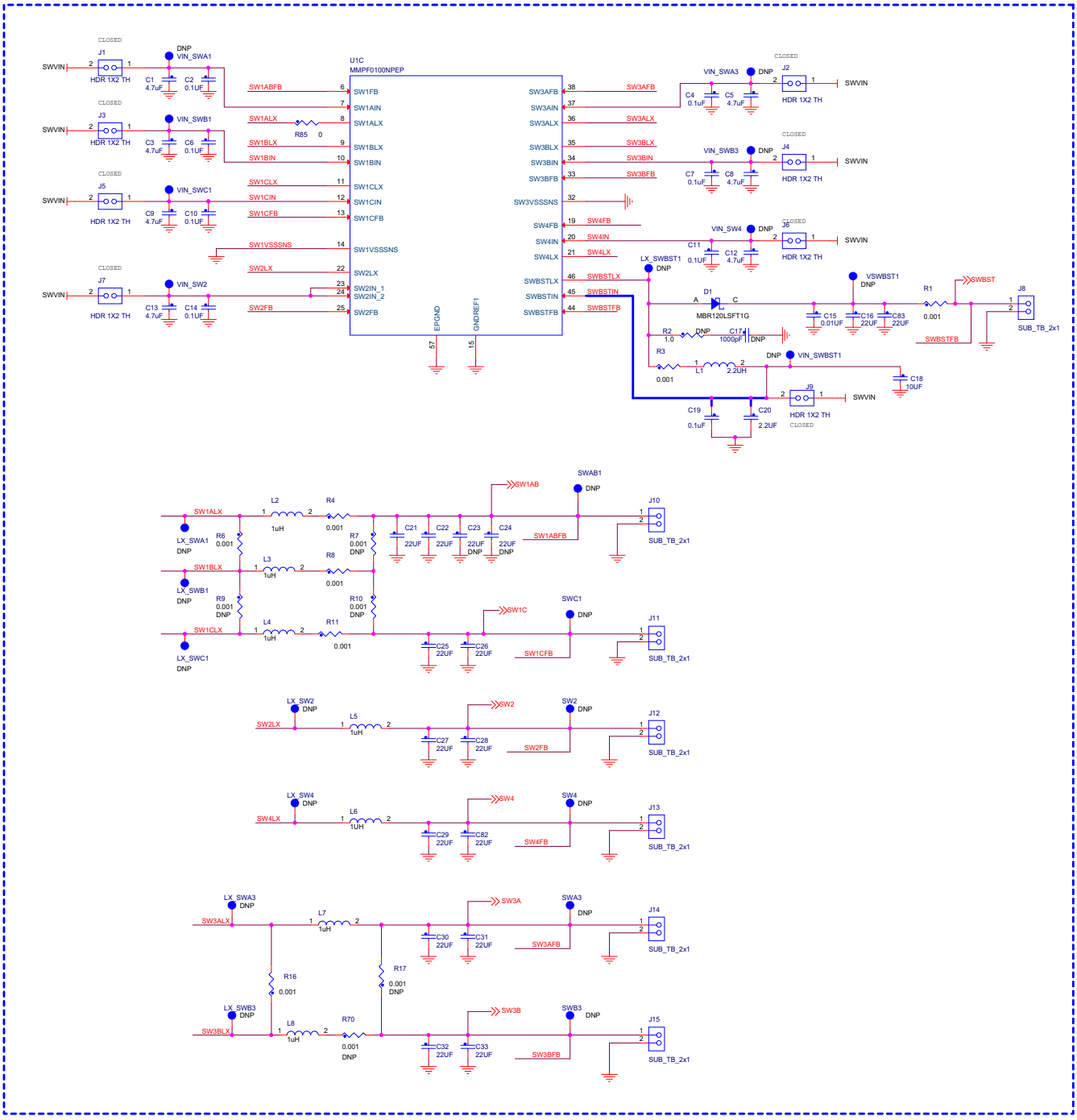


Figure 13. KITPF0100EPEVBE Switching Regulators Schematic

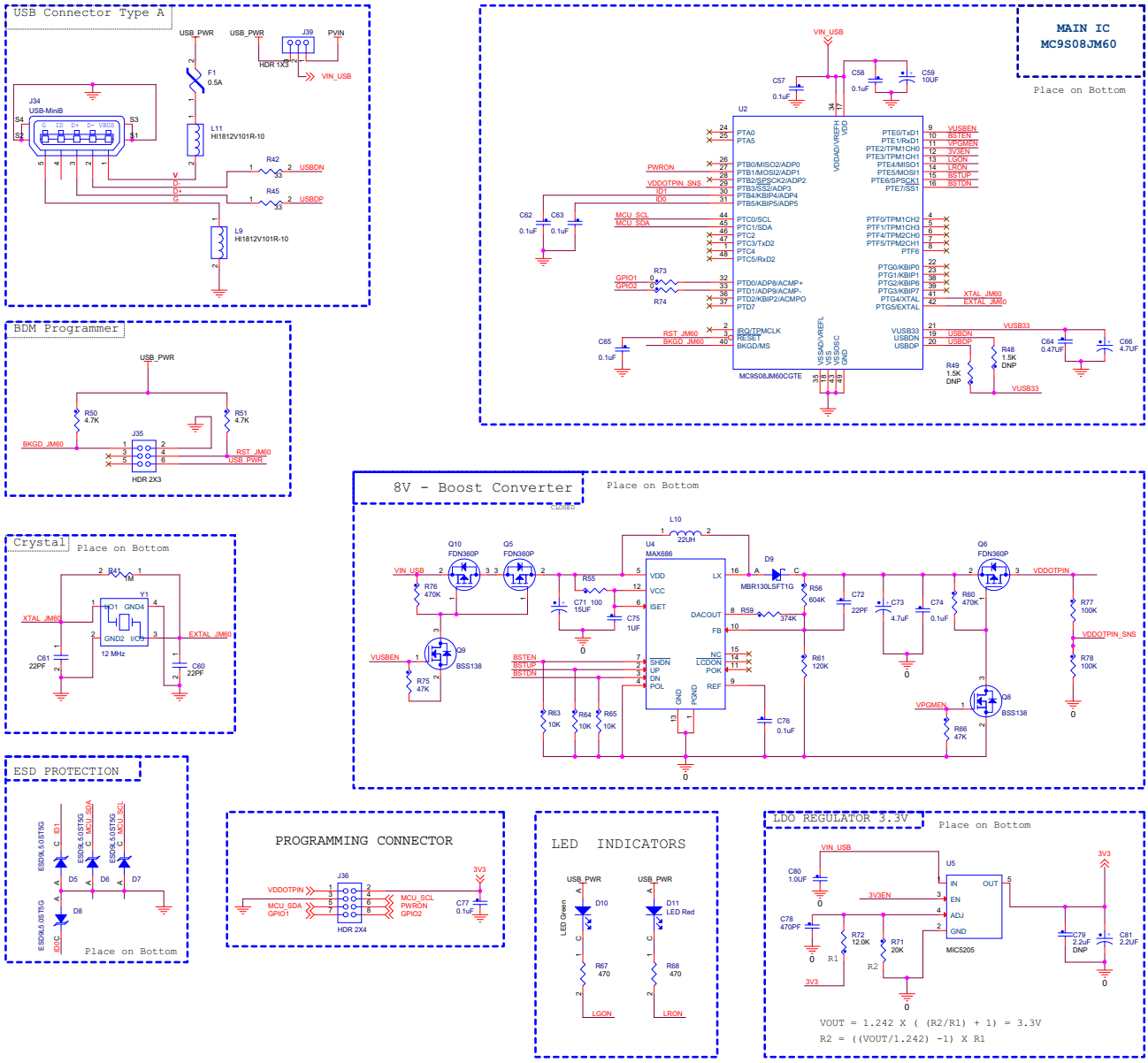


Figure 14. KITPF0100EPEVBE Control/programming Interface Schematic

9 Hardware Description

The KITPF0100EPEVBE operates with a single power supply from 3.1 to 4.5 V and is controlled via USB with help of an integrated USB-I^{2}C communication bridge. By applying the input voltage supply, the KITPF0100EPEVBE will power up according to the default power-up sequence described in the PF0100 datasheet. Furthermore, for controlling the PF0100 device or programming the OTP registers, refer to section Graphical User Interface Description for a detailed description of the KITPF0100GUI software.

Important notice: If power-up sequences and configuration are to be modified, the user must ensure that the register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it will be gated by the buck regulator in the start-up sequence. Refer to the MMPF0100 Datasheet for details on buck regulator setup.

9.1 Jumper Description

Table 1. KITPF0100EPEVBE jumper description

Jumper	Default	Description
J1 - J7	Closed	Buck regulators input power path isolation. Short these jumpers to allow SWxIN to be powered from the SWVIN supply.
J9	Closed	SWBST regulator input power path isolation. Short this jumper to allow SWBSTIN to be powered from the SWVIN supply.
J17	5-6	VDDOTP Supply selector • 1-2: Connect VDDOTP to the OTP Boost output (VDDOTPIN) for OTP programming. • 3-4: Connect VDDOTP to GND to power up from OTP/TBB sequence. • 5-6: Connect VDDOTP to VCOREDIG to power up from Default Power up sequence.
J20	1-2	Coin cell selector. • 1-2: Enables BAT1 as the main coin cell supply. • 2-3: Enables BAT2 as the main coin cell supply.
J40	Closed	Shorts PVIN and SWVIN. Allows supply isolation to provide more accurate efficiency readings on the switching supplies.
J41	Open	Shorts SWVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to SWVIN net. (debugging option)
J27	Closed	Shorts PVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to PVIN net. (debugging option)
J22	2-3	PF0100 input logic supply selector. • 1-2: Connects PF0100 VIN terminal to the 3.3V external LDO regulator for debugging purposes. • 2-3: Connects PF0100 VIN terminal to the main input supply. Refer to Figure 11.
J26	Open	Short to hold PWRON pin low.
J24	Open	Short to pull STANDBY to VSNVS voltage supply.
J30	2-3	I^{2}C pull-up supply selector • 1-2: Pull the SCL/SDA signals to the external 3.3V LDO regulator output. • 2-3: Pull the SCL/SDA signals to the selected VDDIO supply. If 3.3V LDO output is desired as the VDDIO and I^{2}C supply, remove R33 and R34 and short pins 1,2 and 3 to make sure VDDIO uses the same reference as the I^{2}C supply.
J39	1-2	Control Interface input supply selector • 1-2: Enables PVIN node as the input supply source for the control interface. • 2-3: Enables USB power as the input supply source for the control interface.

9.2 Connectors and Terminal Blocks Description

Table 2. Terminal Blocks descriptions

Connector	Function	Pin definition
J8	SWBST	Pin 1 - SWBST Output Pin 2 - GND
J10	SW1AB	Pin 1 - SW1AB Output Pin 2 - GND
J11	SW1C	Pin 1 - SW1C Output Pin 2 - GND
J12	SW2	Pin 1 - SW2 Output Pin 2 - GND
J13	SW4	Pin 1 - SW4 Output Pin 2 - GND
J14	SW3A	Pin 1 - SW3A Output Pin 2 - GND
J15	SW3B	Pin 1 - SW3B Output Pin 2 - GND
J16	VGEN1/VGEN2	Pin 1 - VGEN1 Output Pin 2 - GND Pin 3 - VGEN2 Output
J18	VGEN3/VGEN4	Pin 1 - VGEN3 Output Pin 2 - GND Pin 3 - VGEN4 Output
J19	VGEN5/VGEN6	Pin 1 - VGEN5 Output Pin 2 - GND Pin 3 - VGEN6 Output
J21	VSNVS/VREFDDR	Pin 1 - VSNVS Output Pin 2 - GND Pin 3 - VREFDDR Output
J25	Main Input Supply	Pin 1 - GND Pin 2 - PVIN Pin 3 - SWVIN
J29	Interfacing 1	Pin 1 - INTB Pin 2 - SDWNB Pin 3 - RESETBMCU
J32	Interfacing 2	Pin 1 - STANDBY Pin 2 - PWRON Pin 3 - GND
J31	I^2C Signals	Pin 1 - SCL Pin 2 - SDA
J33	VDDIO	Pin 1 - VDDIO Pin 2 - GND

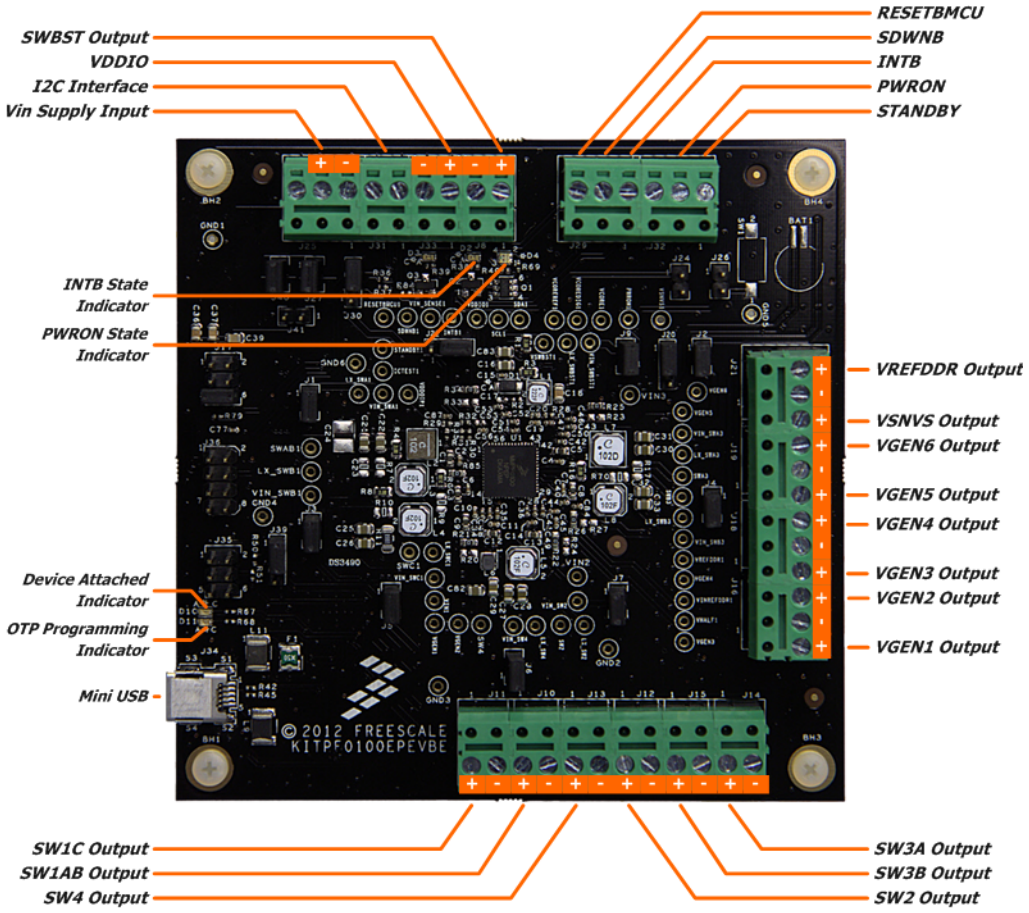
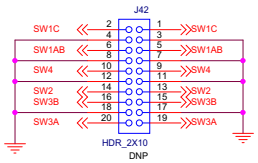
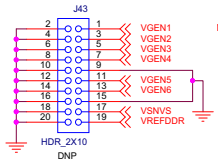
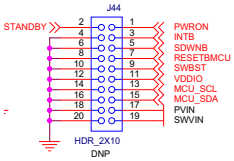


Figure 15. Input/Output Terminal Blocks

Table 3. Connector Description

Connector	Function	Pin definition
J34	Mini USB connector	Pin 1 - VBUS Pin 2 - D- Pin 3 - D+ Pin 4 - NC Pin 5 - GND Chassis - GND
J35	BDM connector	Pin 1 - BKGD_JM60 Pin 2 - GND Pin 3 - NC Pin 4 - RST_JM60 Pin 5 - NC Pin 6 - USB_PWR
J36	Programmer connector	Pin 1 - VDDOTPIN (8.5V boost output) Pin 2 - 3V3 (3.3 V LDO output) Pin 3 - GND Pin 4 - MCU_SCL (I^2C clock signal) Pin 5 - MCU_SDA (I^2C data signal) Pin 6 - PWRON (Controls the PWRON on the target device) Pin 7 - GPIO 1 (General Purpose GPIO) Pin 8 - GPIO 2 (General Purpose GPIO)
J42	Debug Port 1	Debugging connector for future development tools. 
J43	Debug Port 2	Debugging connector for future development tools 
J44	Debug Port 3	Debugging connector for future development tools 

9.3 Debug and Configuration Components

The KITPF0100EPEVBE allows full flexibility to change the default configuration of SW1A/B/C and SW3A/B outputs to one more suitable for a specific application scenario. It also provides several source options for the LDO supplies to test various loading and supplying scenarios.

Test point are provided on key nodes of the KITPF0100EPEVBE to allow full debugging capability during application development.

9.3.1 SW1A/B/C Configuration Components

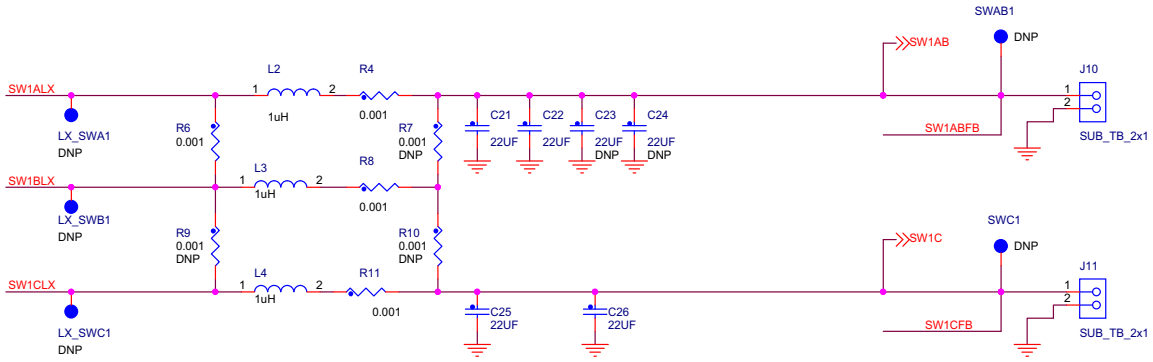


Figure 16. SW1A/B/C Output Configuration

The SW1A/B/C regulator can be configured in various operating modes as described in Table 4.

Table 4. SW1ABC Configuration Chart

Component	SW1A/B/C Single phase	SW1A/B Single phase SW1C independent	SW1A/B Dual phase SW1C independent
R6	Closed	Closed	DNP
R9	Closed	DNP	DNP
R4	Closed	Closed	Closed
R7	Closed	DNP	Closed
R8	DNP	DNP	Closed
R10	Closed	DNP	DNP
R11	DNP	Closed	Closed
L2	1.0 µH ISAT = 6.0 A	1.0 µH ISAT = 4.5 A	1.0 µH ISAT = 2.4 A
L3	N/A	N/A	1.0 µH ISAT = 2.4 A
L4	N/A	1.0 µH ISAT = 2.4 A	1.0 µH ISAT = 2.4 A

9.3.2 SW3A/B Configuration Components

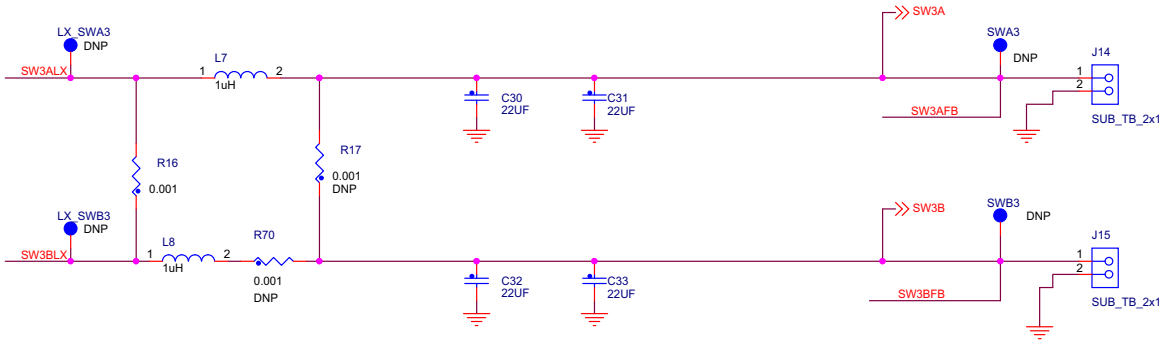


Figure 17. SW3A/B Output Configuration

The SW3A/B regulator can be configured in various operating modes as described in Table 5.

Table 5. SW3ABC Configuration Chart

Component	SW3A/B Single phase	SW3A/B Dual phase	SW3A Independent SW3B Independent
R16	Closed	DNP	DNP
R17	Closed	Closed	DNP
R70	DNP	Closed	Closed
L7	1.0 µH ISAT = 3.9A	1.0 µH ISAT = 3.0A	1.0 µH ISAT = 3.0 A
L8	N/A	1.0 µH ISAT = 3.0 A	1.0 µH ISAT = 3.0 A

9.3.3 LDO Input Supply Source Selection

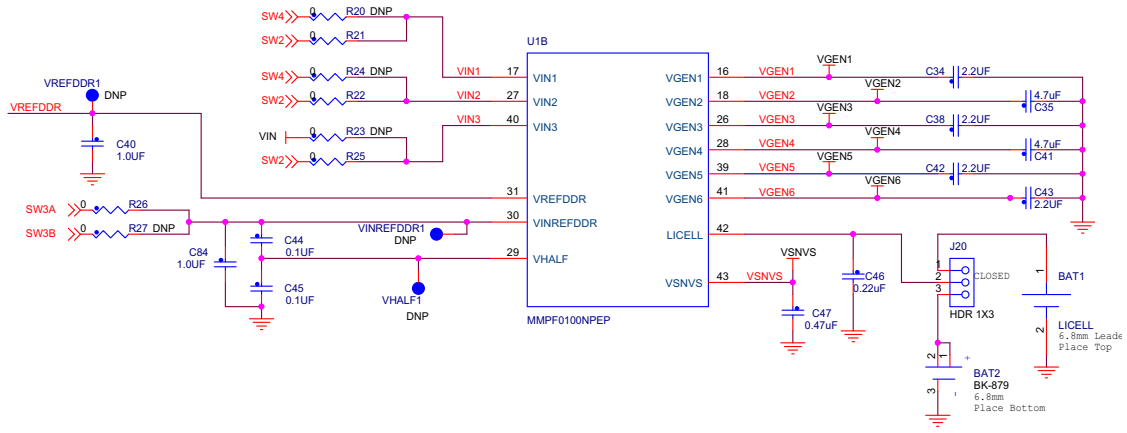


Figure 18. LDO Schematic Configuration

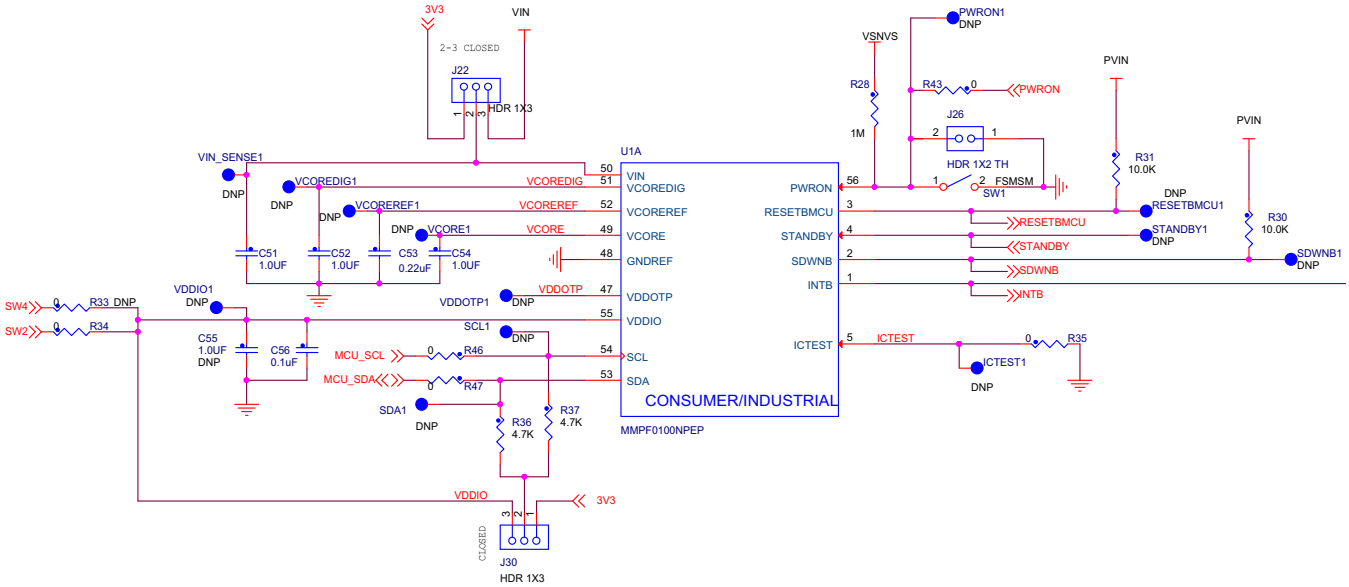


Figure 19. Logic and Core Supplies Schematic

Table 6. LDO Input Supply Configuration Chart

Input Pin	Input options
VIN1	Input supply for VGEN1 and VGEN2 R20 = SW4 R21 = SW2
VIN2	Input supply for VGEN3 and VGEN4 R24 = SW4 R22 = SW2
VIN3	Input supply for VGEN5 and VGEN6 R23 = VIN R25 = SW2
VINREFDDR	VREFDDR input supply R26 = SW3A R27 = SW3B
VDDIO	VDDIO Input supply R33 = SW4 R34 = SW2

1. Make sure to populate only one option per input pin to avoid shorts between various sources.

9.3.4 Test point

All test points are clearly marked on the KITPF0100EPEVBE evaluation board. Figure 20 shows the location of various test points of interest during evaluation.

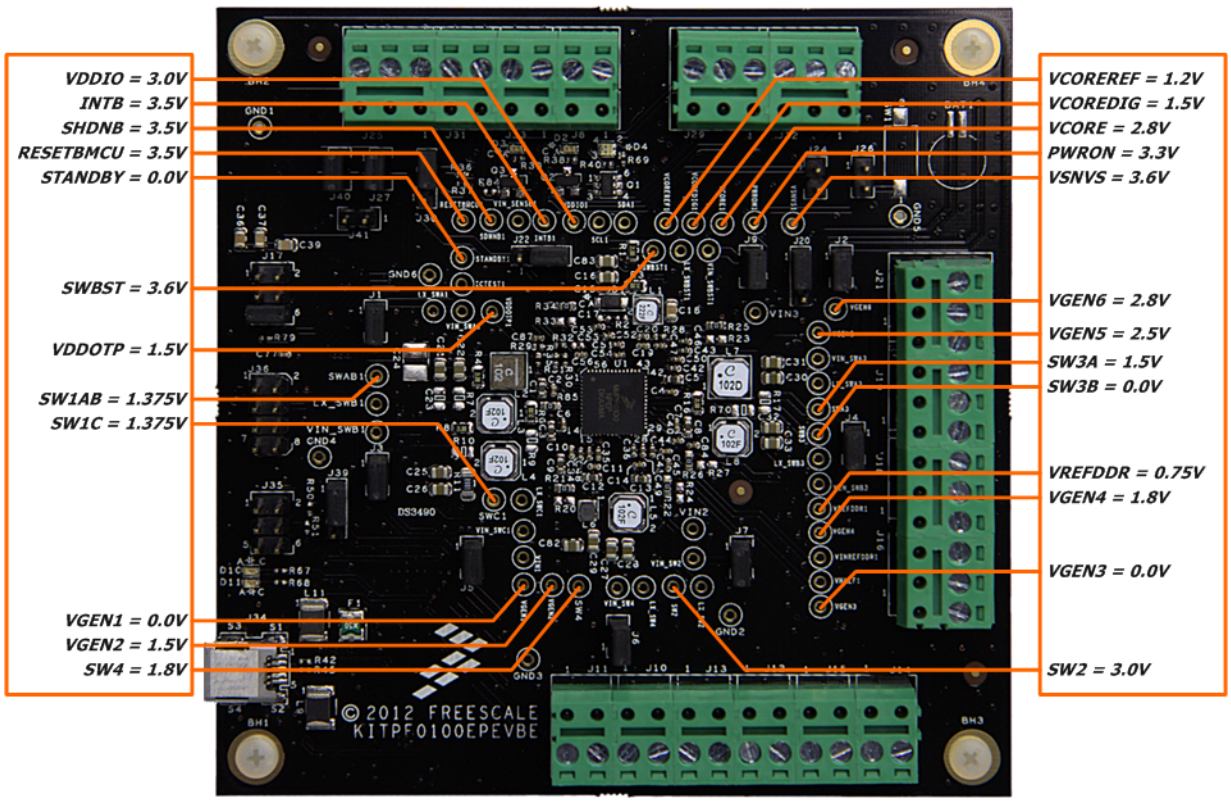


Figure 20. Key Test Point Locations and Default Voltages

9.4 Miscellaneous Components

9.4.1 Power on Push Button

A footprint for a normally open, momentary push-button is provided at the PWRON terminal to allow a momentary low state by pressing the push button. R43 allows isolation of the PWRON terminal from the MCU GPIO controlling this pin.

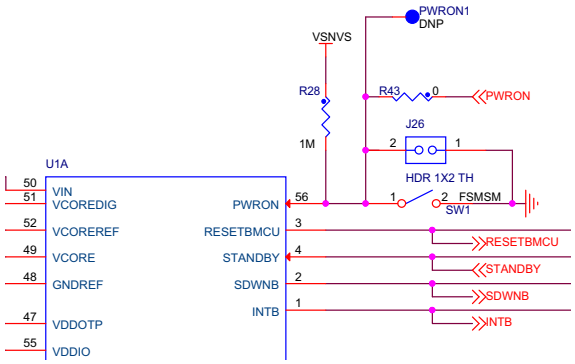


Figure 21. Power on Circuit

9.4.2 PMIC LED Indicators

LED indicators are provided to notify the PMIC status to the user. Figure 22 shows the PMIC status LEDs D2 and D4, and a Reserved LED indicator D3, that allows for an external rework connection to the transistor gate if any given signal debug is required.

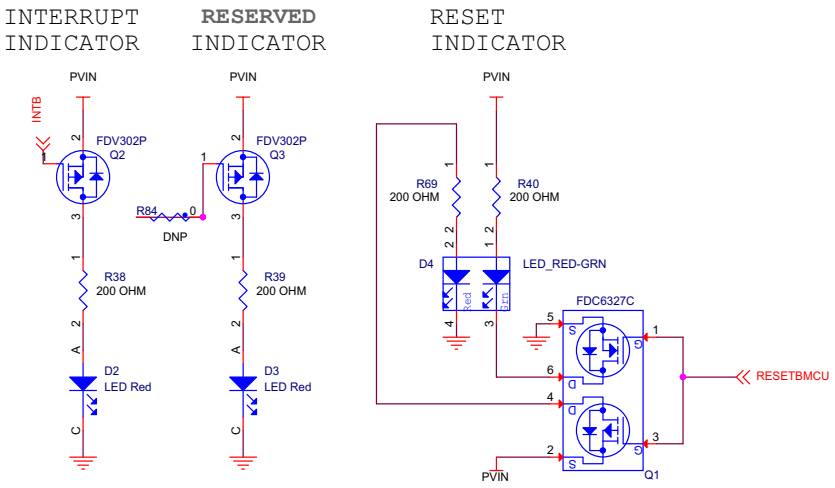


Figure 22. PMIC Status Indicator

Table 7 describes the meaning of the LED states.

Table 7. LED State Description

LED	Description
D2	Interrupt Notification ON = PMIC has detected an unmasked interrupt OFF = No interrupt detected
D4	RESETBMCU Notification Green = PMIC is in regulation and operating properly Red = PMIC is out of regulation
D3	Reserved debug LED ON = Q3 gate (R84 pad) is low OFF = Q3 gate (R84 pad) is high or floating

9.4.3 Control/Programming Interface

This onboard USB-to-I^{2}C interface comprises three basic blocks.

1. Controlling MCU (MC9S08JM60CGTE) for USB-I^{2}C translation.
2. 3.3V LDO supply for external device controlling.
3. 8.25V boost converter for OTP programming.

The control/programming interface allows one to program the onboard PF0100 PMIC. Alternatively, the interface can serve as a programmer for external devices though the connector J36.

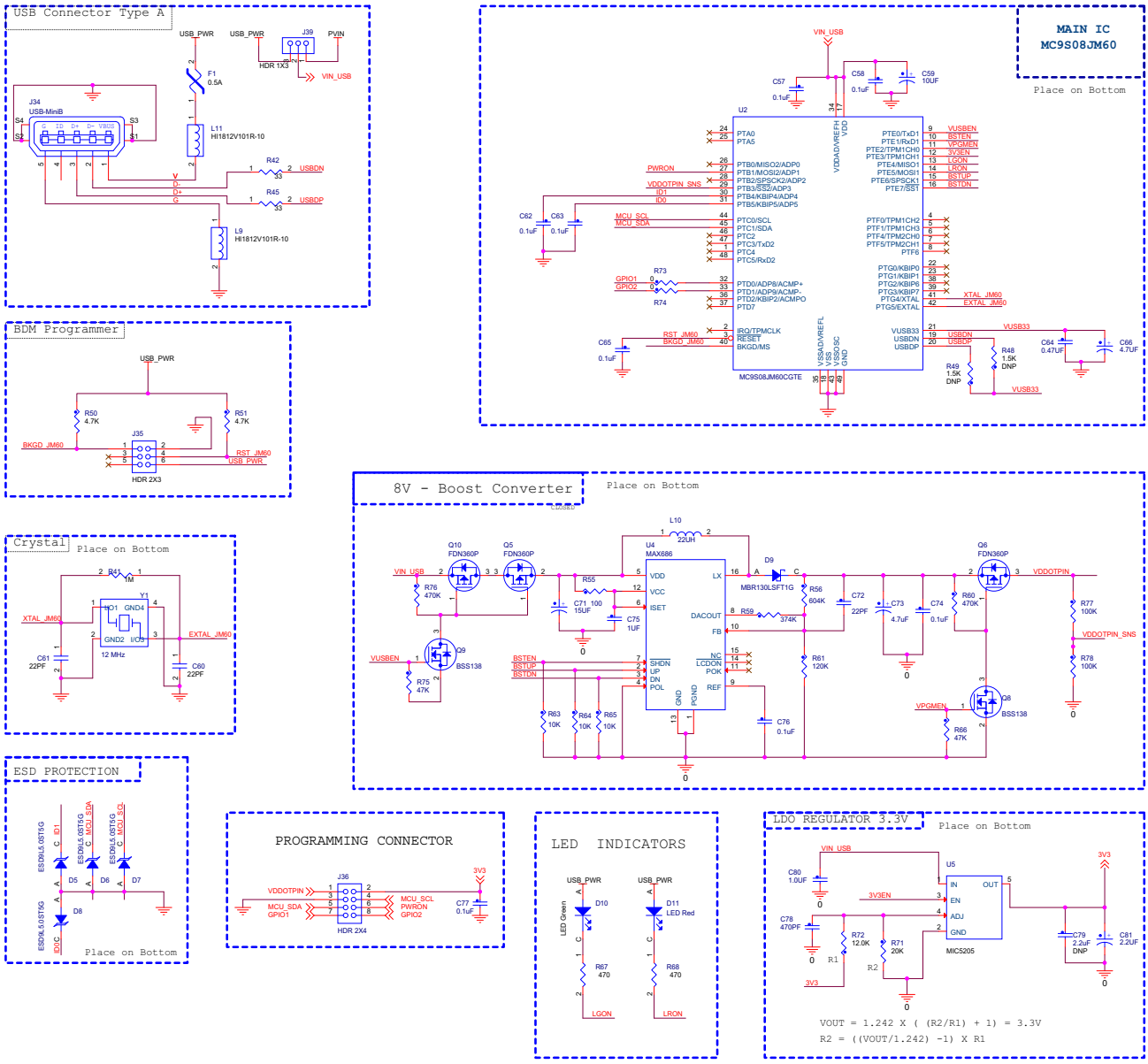


Figure 23. Control/Programming Interface Schematic

10 Graphical User Interface Description

The KITPF0100 GUI is based on a tabbed interface. Each tabs can be selected to display a window associated with one functional aspect of the PF0100 device.

10.1 Getting Started

1. Supply 3.6V to J25 of the EVK board, then connect the USB cable from the USB-MiniB port (J34) to the computer. J30 should be in position (2-3); otherwise, you will receive an error message.
2. Press the “Open Session” button to search for the PF Programmer device.
3. The “Select Resource” dialog box should pop up, and you should see the KITPF0100EPEVBE device listed. The USB Vendor ID is 0x15A2, and the Part ID is 0x00F5 for the KITPF0100EPEVBE.

Select the device and press the “OK” button.

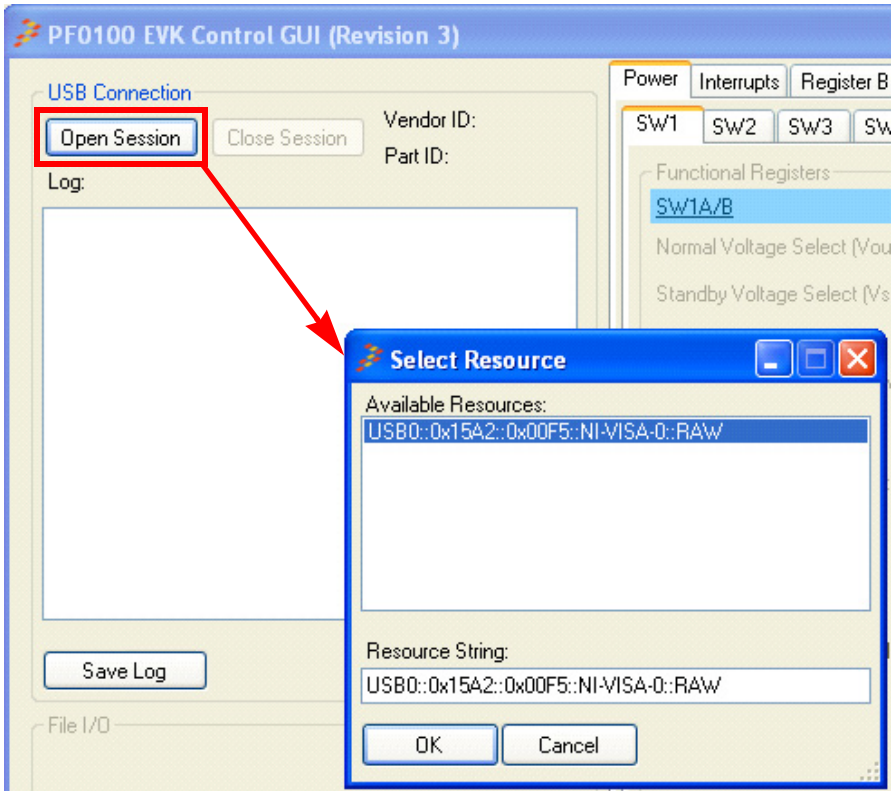


Figure 24. OPEN USB Connection

4. The “Select Resource” dialog should close, and the Log List will display a message that you are connected to the KITPF0100EPEVBE. The Vendor ID and Part ID will also be displayed to let you know that you are connected to the right device.
   - The Log List can be saved to a text file at any time by pressing the “Save Log” button, and a "File Save” dialog box will pop up.
   - The Log List can also be cleared at any time by pressing the “Clear Log” button.

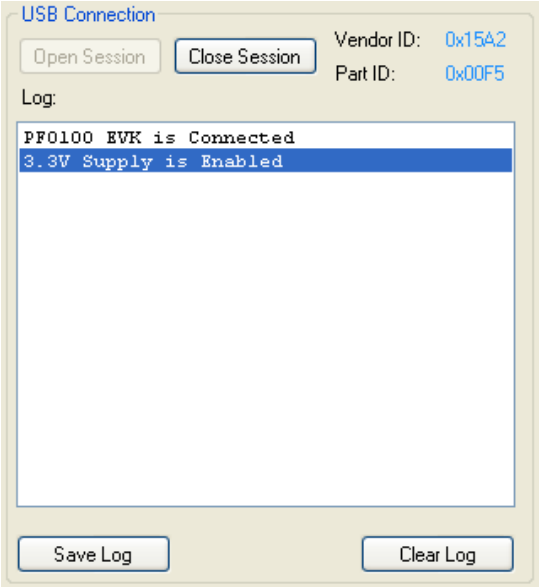


Figure 25. Log List Box.

5. If prototyping is desired, the Try-Before-Buy mode can be enabled or disabled though the TBB On or TBB Off buttons respectively. The operating mode will be displayed on the lower left area of the KITPF0100GUI as shown in Figure 26. The KITPF0100GUI version is shown in the lower right area of the graphical interface.

Figure 26. TBB Mode Enable/Disable

6. **This step is optional**: To use the onboard 3.3V LDO to supply VDDIO and the pull-up source for I^2C signal lines instead of the SW2 regulator of PF0100. Put J30 in position [1-2] and press the “Enable 3.3V Supply” button.

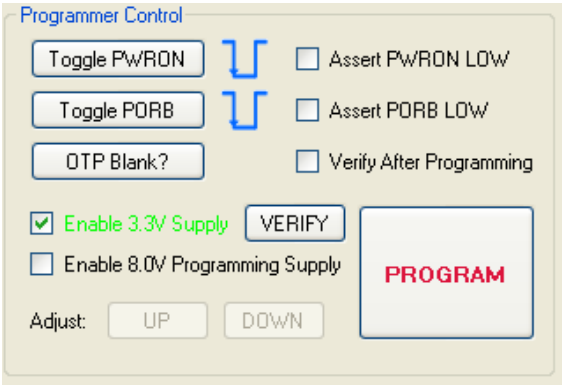


Figure 27. 3.3V Supply Enable

10.2 Verify I²C Communication to PF0100

Use the “Byte Write” button to write one byte of data to register 0x1C of PF0100 and use the “Byte Read” button to read back register content at address 0x1C to verify correct data was written. The Log List should also reflect what I²C transactions the GUI has processed.

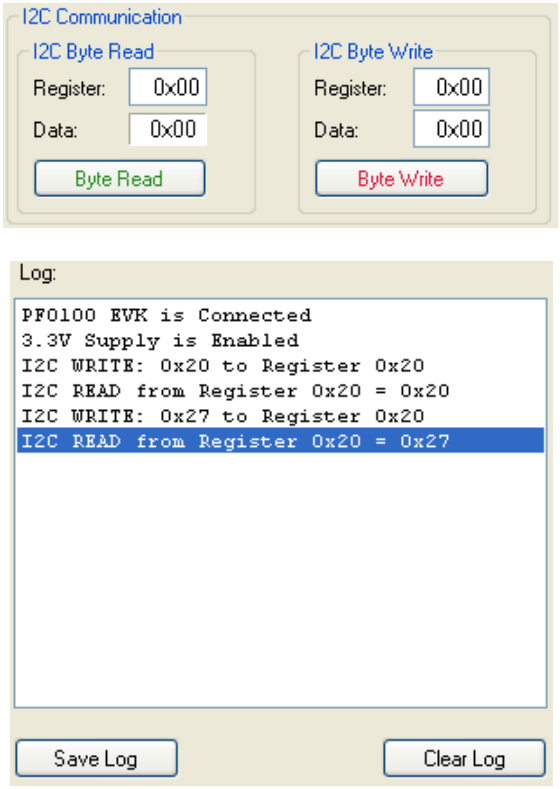


Figure 28. Verify I²C Communication.

10.3 GUI Features

There are five functional tabs in the KITPF0100GUI to allow programming the PF0100 registers. They also permit one to perform either prototyping or One-Time Programming (OTP) of the fuse registers.

The *Power* tab provides user access to control both the switching as well as the linear regulators on PF0100.

The switching regulators can be programmed by sub-tabs for SW1, SW2, SW3, SW4, and SWBST. For each of these tabs, the user has access to functional registers that configure the output voltage, the standby voltage, the off-mode voltage, the phase control, the switching frequency and more. The user can also configure the OTP register via the bottom half of the tab, which selects the start-up sequence of the switching regulators as well as phase configuration for SW1 and SW3.

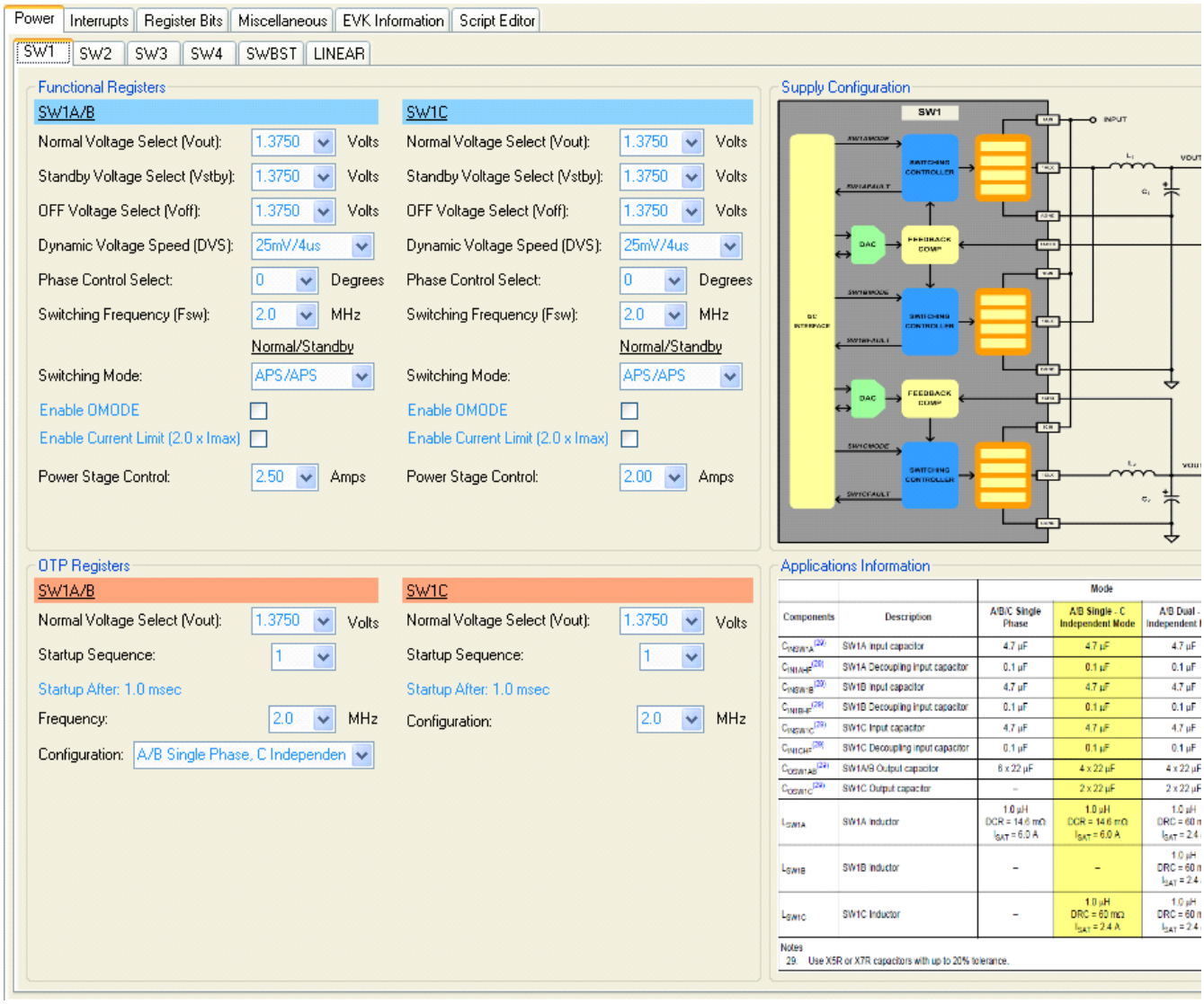


Figure 29. Switching Regulators Tab

Linear regulators can be programmed using the LINEAR sub-tab. It enables the user to control the output voltage and the start-up sequence of the regulators as well as to choose between the standby and low power mode.

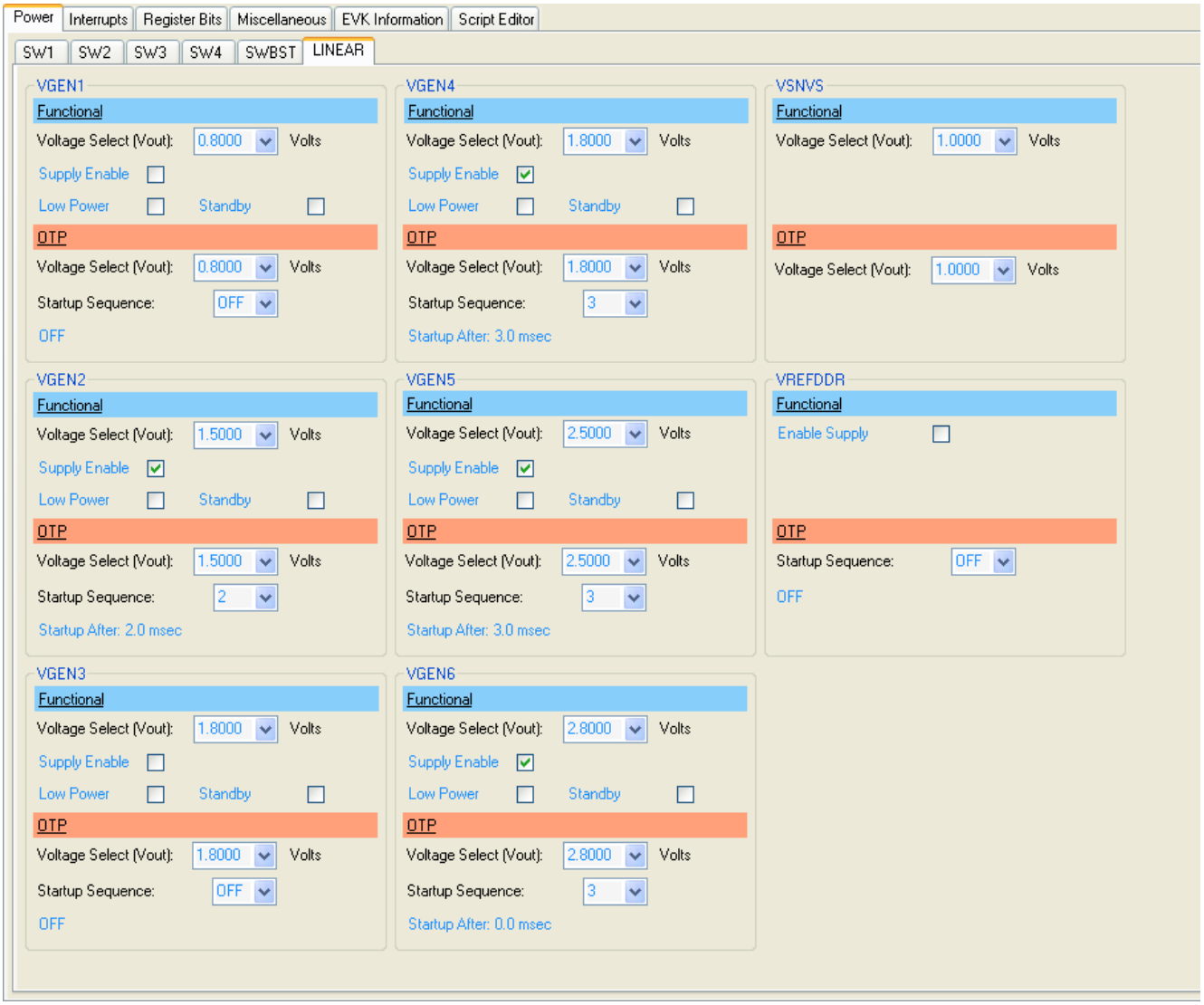


Figure 30. LDO Regulators Tab

The *Interrupts* tab provides user access to the four interrupt registers in PF0100 functional register map. The user can choose to read the interrupts by pressing on the “Read Interrupt x” button.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a "1" to the appropriate bit in the Interrupt Status register; this will also cause the INTB pin to go high.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin will not go low. A masked interrupt can still be read from the Interrupt Status register.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and neither latched nor clearable.

The user may choose to press the “Poll Interrupt x” control to read the *Interrupts* tab every 500ms.

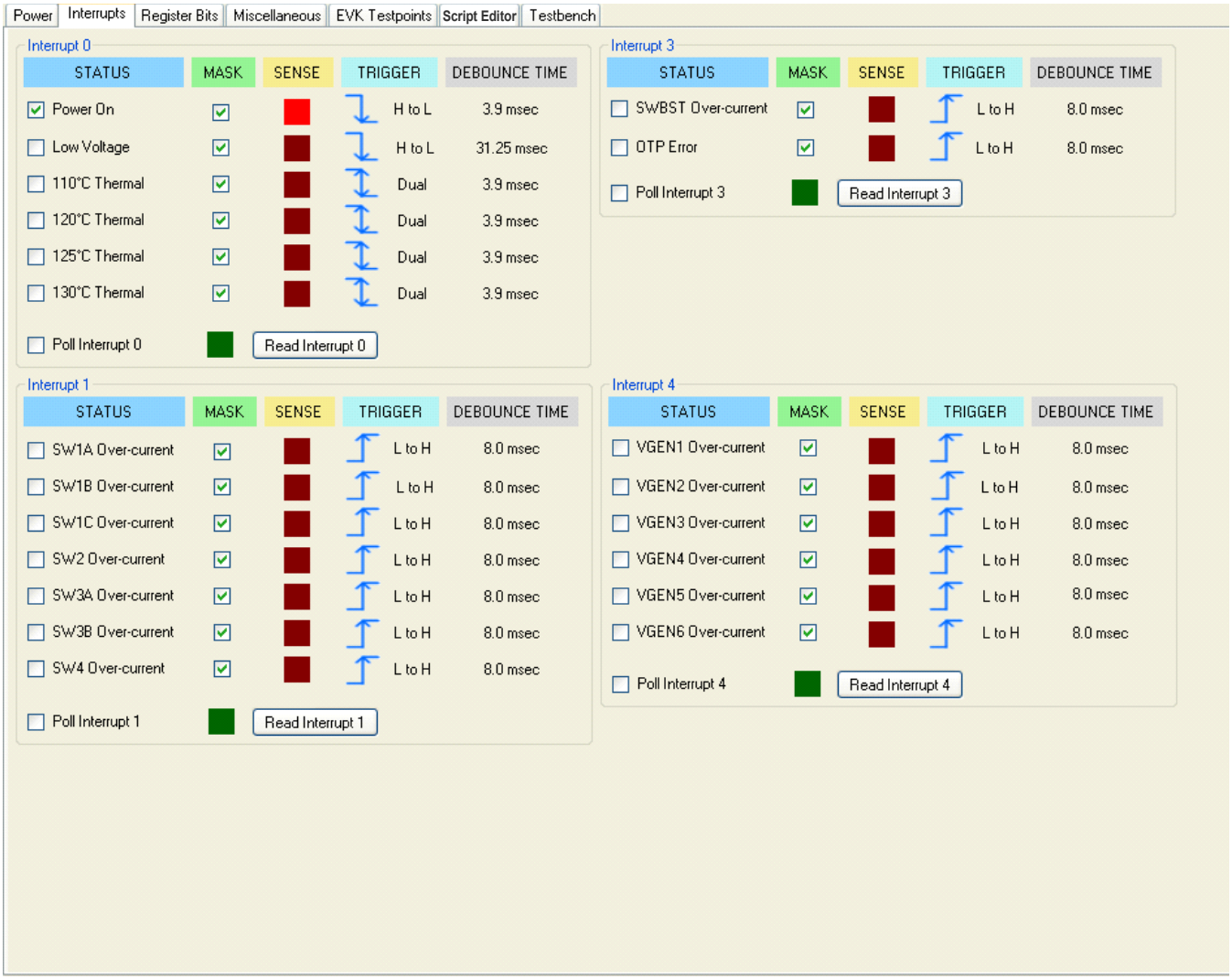


Figure 31. Interrupts Tab

The *Register Bits* tab allows bit programming of the PF0100 registers. This is an alternative to the I^2C single byte write and read controls shown in section "Verify I2C Communication to PF0100".

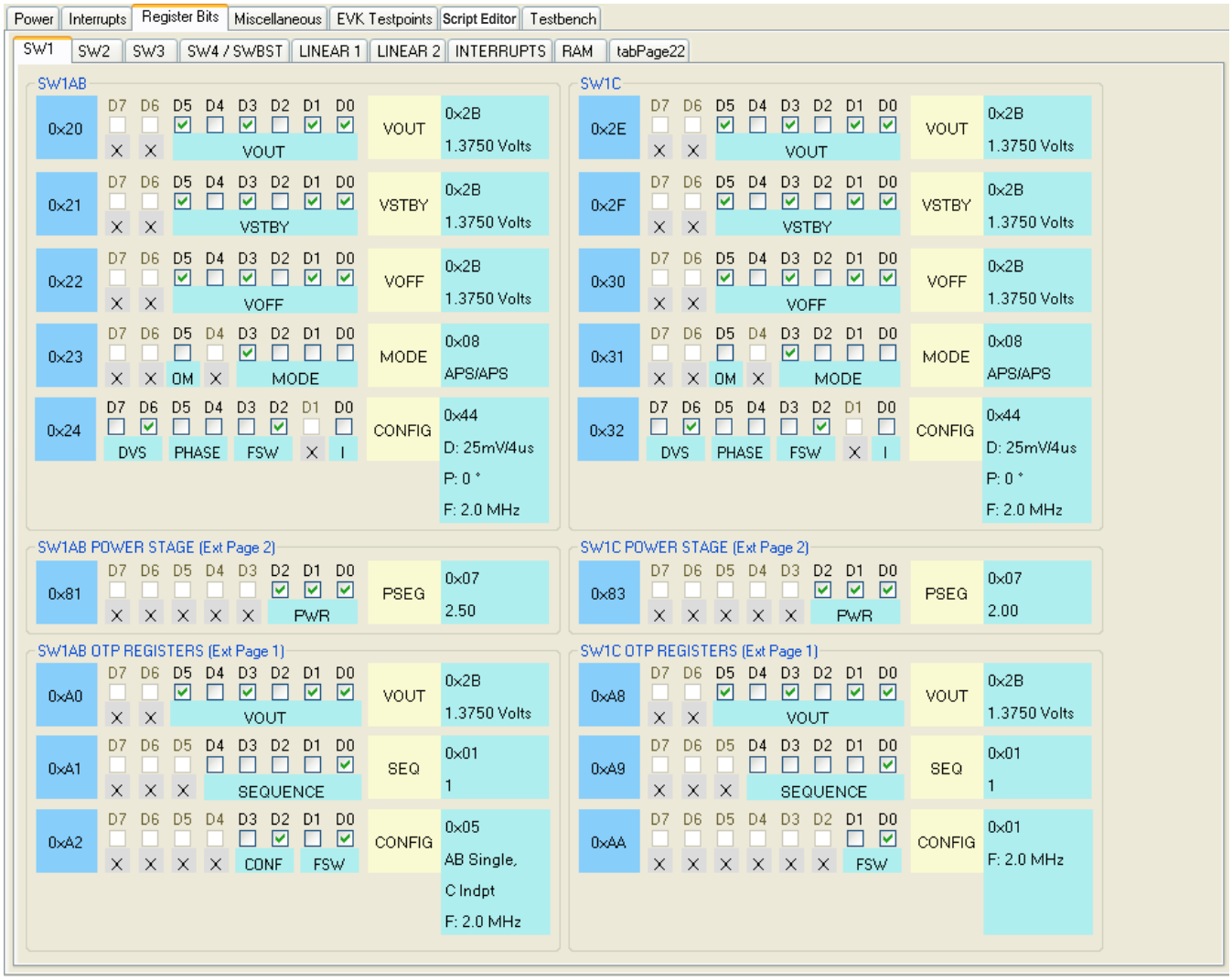


Figure 32. Register Bits Tab

The *Miscellaneous* tab allows the user to read the silicon device ID, configure the coin cell charger, enable LDO short-circuit protection, set the de-bounce time of logic IO, and communicate with memory registers A-D.

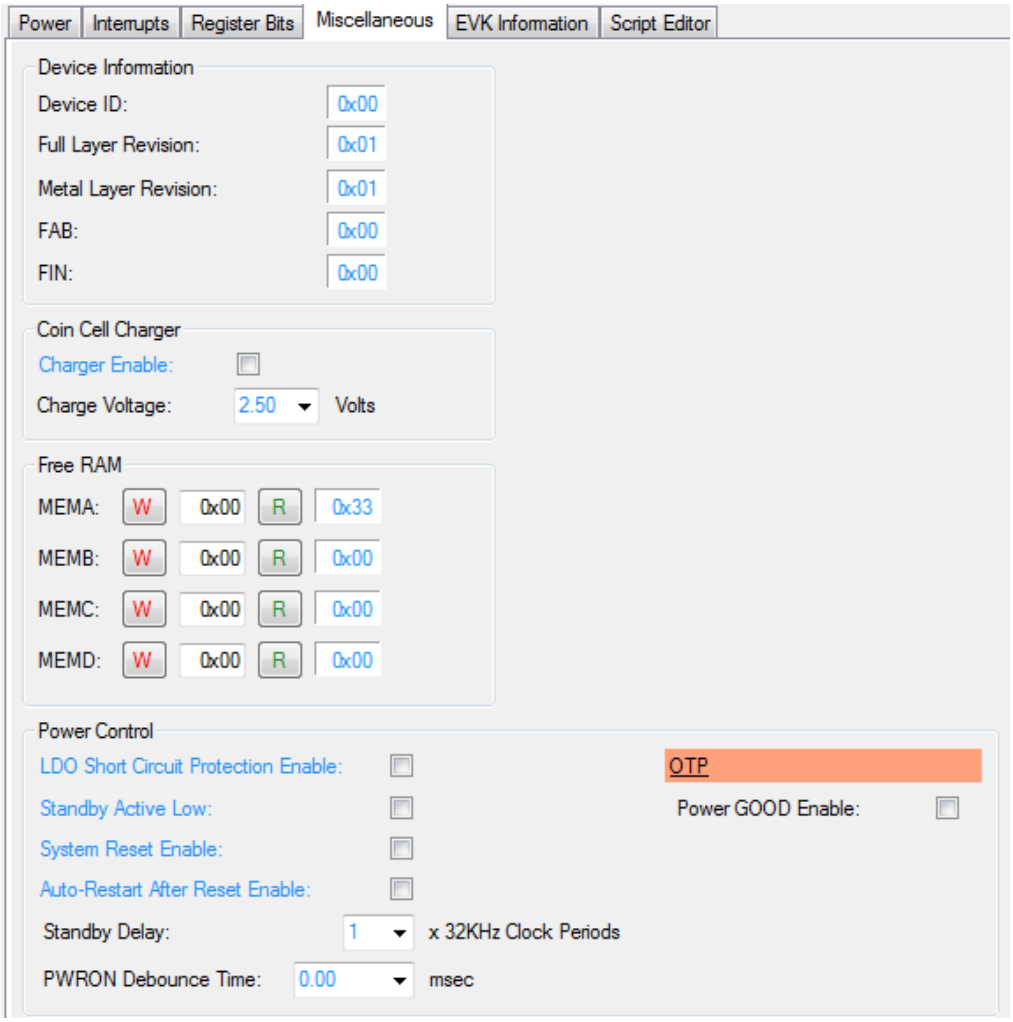


Figure 33. Miscellaneous Tab

The *EVK Test Points* tab provides a visual aid to the top layer of KITPF0100EPEVBE.

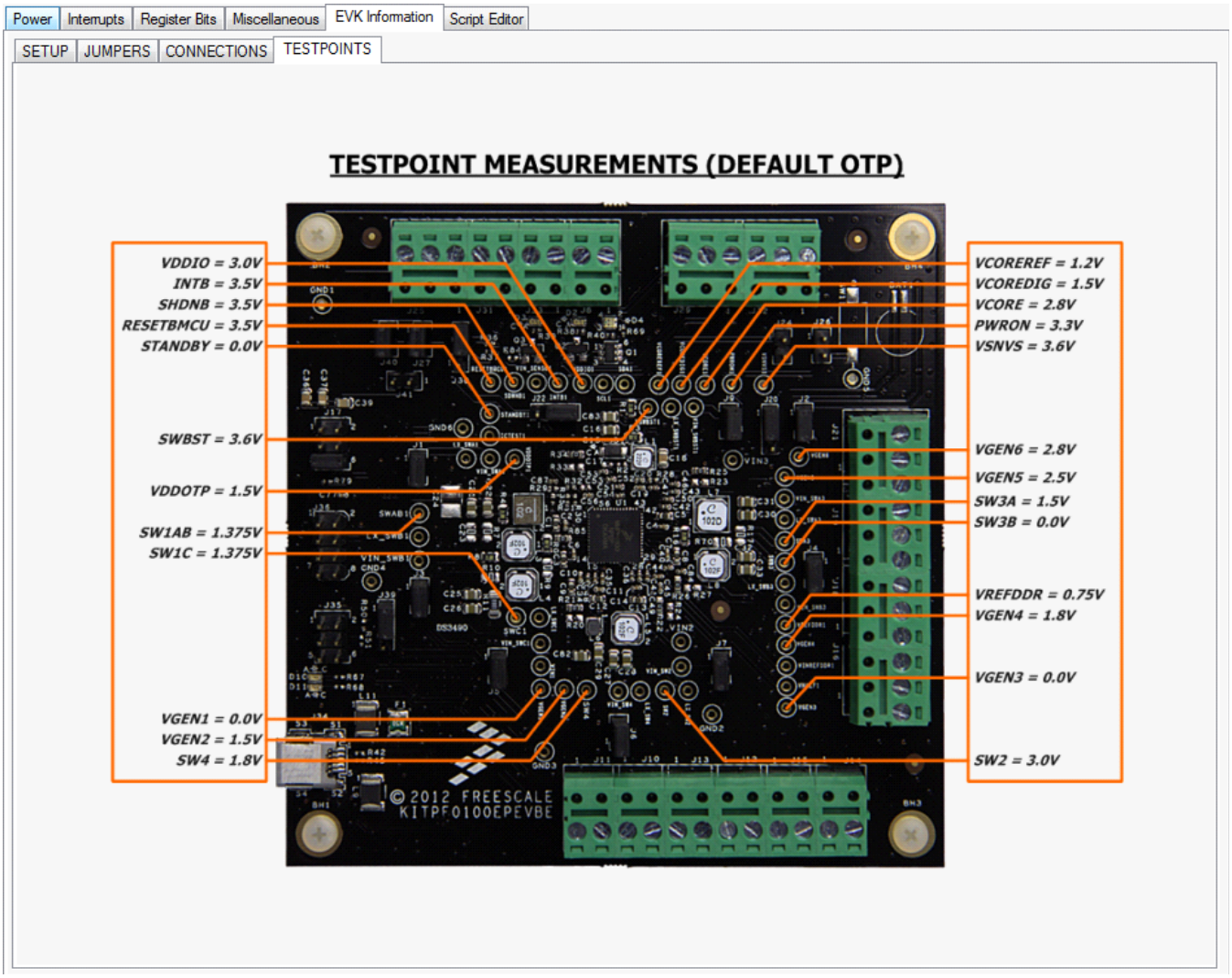


Figure 34. EVK Test Point Tab

The *Script Editor* Tab allows one to create, load and save configuration scripts for the PF0100 device. For more information on how to create a configuration script, see section “Using the Script Editor”.

10.4 Using the Script Editor

The Script Editor is a powerful tool that automates the PF0100 development process. Scripts are groups of commands that are executed sequentially. They can quickly load PF0100 registers with your desired configuration, or they can help you to determine the correct power-up sequence for your design. Scripts are stored as simple text files, and as such, can be edited with any text editor. Since scripts are driven by your PC, PMIC configurations can be explored and validated prior to connecting to a host i.MX processor.

The Script Editor work area is shown in Figure 35. Script files are created in the large work area to the left. The blank area to the right-hand side is the Script Log, which displays the script output as it steps sequentially.

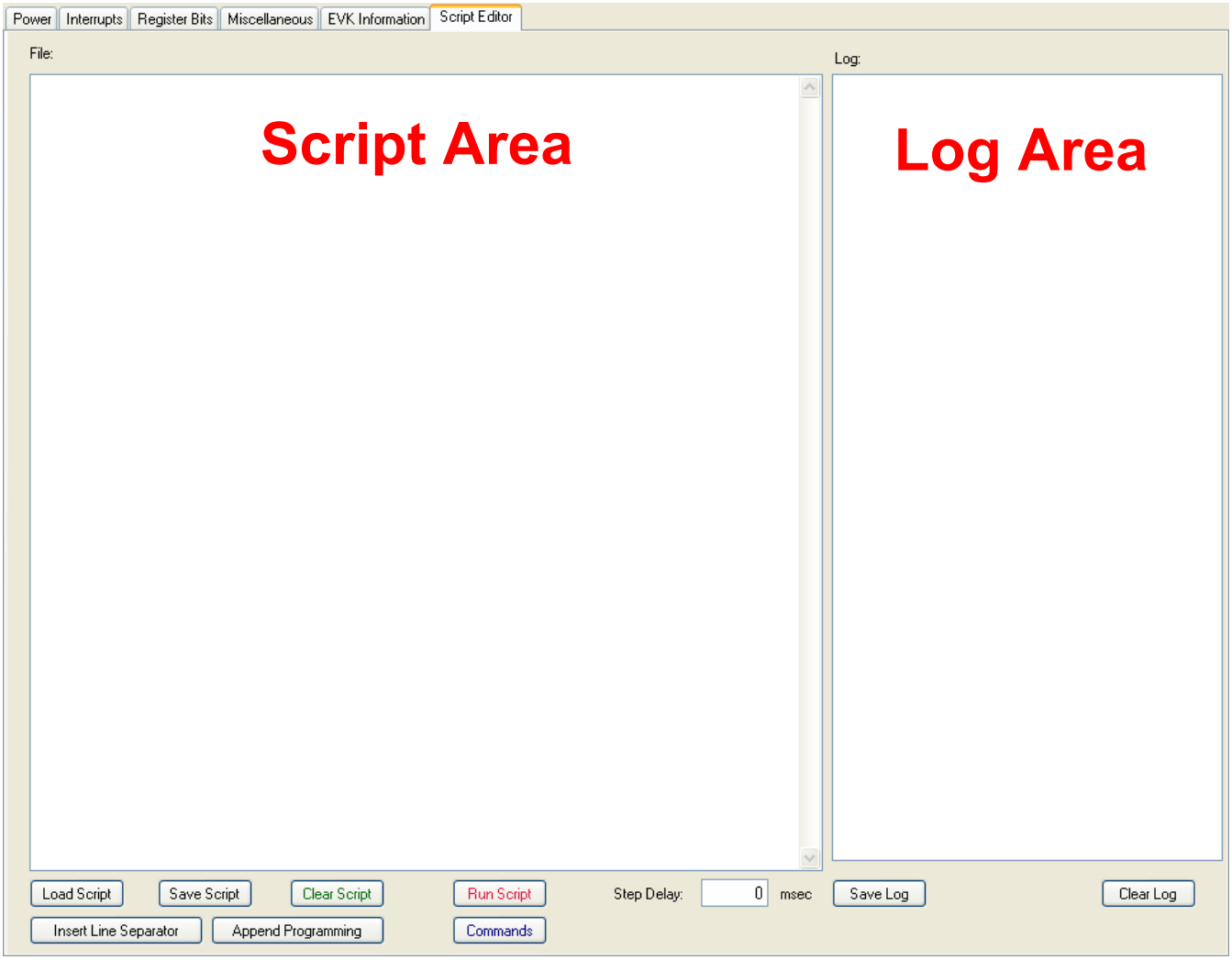


Figure 35. Script Editor Window

The following list describes all the available buttons on the Script Editor tab.

- **Load Script:** Launches the “File Load” dialog box allowing the user to select and load a stored script file.
- **Save Script:** Launches the “File Save” dialog box, allowing the user to save a script file to storage.
- **Clear Script:** Clears the current Script Editor work area to prepare for writing a new script.
- **Run Script:** Begins execution of the currently loaded script. Execution runs sequentially.
- **Step Delay:** Entered as an integer number between 0 and 1000 milliseconds. Double-click with the left mouse button over the text box to begin editing the value, then press the Enter key.
- **Insert Line Separator:** Inserts a comment at the current cursor position that represents a separating line. Used to organize long scripts.
- **Append Programming:** Inserts all the commands required to program the OTP memory into the Script Editor at the current cursor location.
- **Save Log:** Launches the “File Save” dialog box, allowing users to save the Script Log to a file.
- **Clear Log:** Clears the Script Log.
- **Commands**: Displays the pop-up window shown in Figure 40, with a graphical set of commands to add to the script.

10.4.1 Loading and Running a Script

To load a preexisting script file, press the “Load Script” Button. The “File Load” dialog box will appear, allowing you to navigate to the directory where your script file is located. Select the file you want and press the “Open” button.

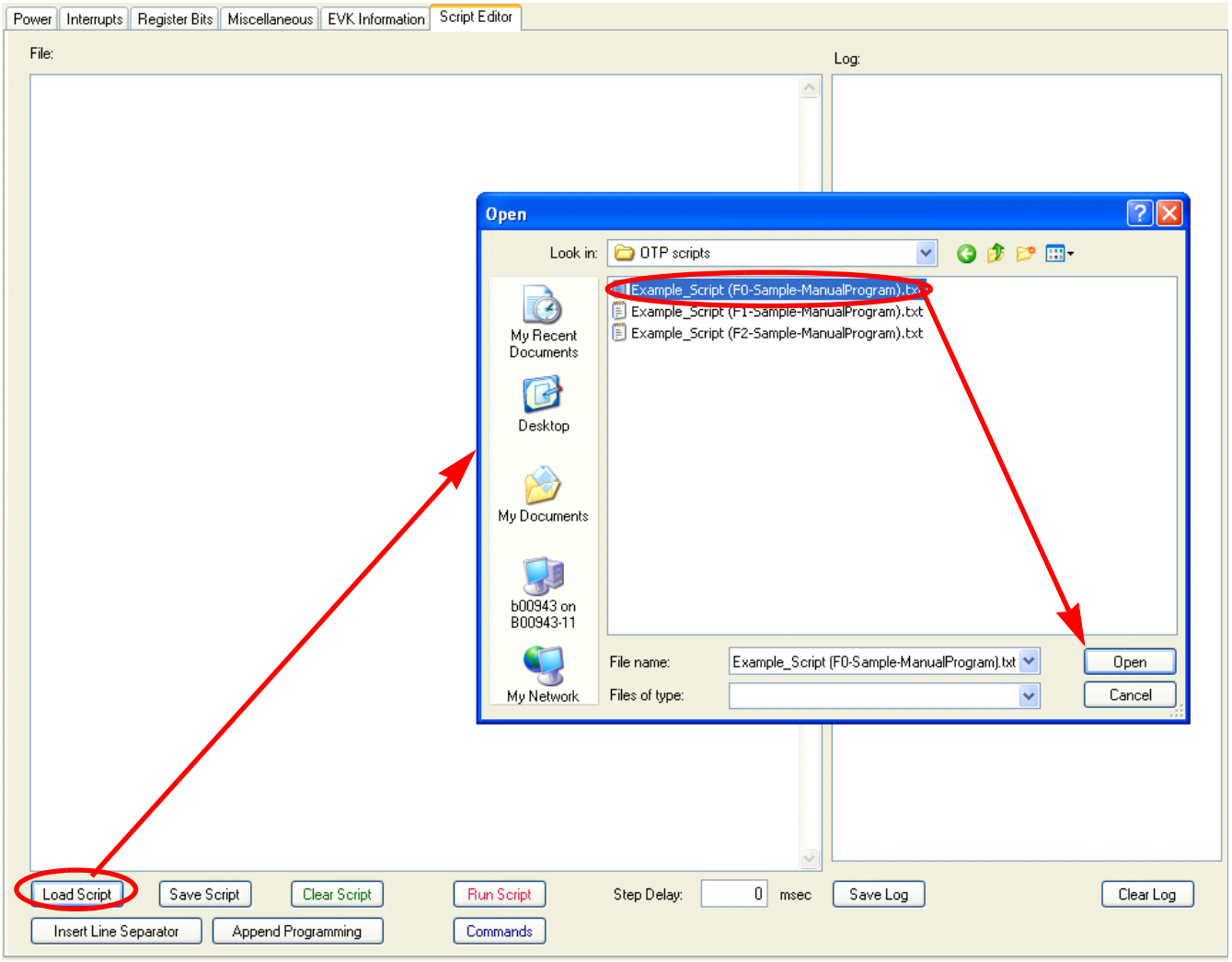


Figure 36. Loading a Script File

The Script Editor work area will now be filled with the file content, and the file name will appear next to the "File:" label and also as an entry in the Script Log.

Next, change the script's Step Delay to allow delay between each command. For instance, 50 ms are used in the example shown in Figure 37. To make this change, double-click with the left mouse button while pointing to the "Step Delay" text box. The text box background color will turn pink, indicating the value is being changed, but has not yet been updated. Enter the desired delay value, and press the Enter key. Notice that the text box background color returns to white, indicating that your updated value has been accepted.

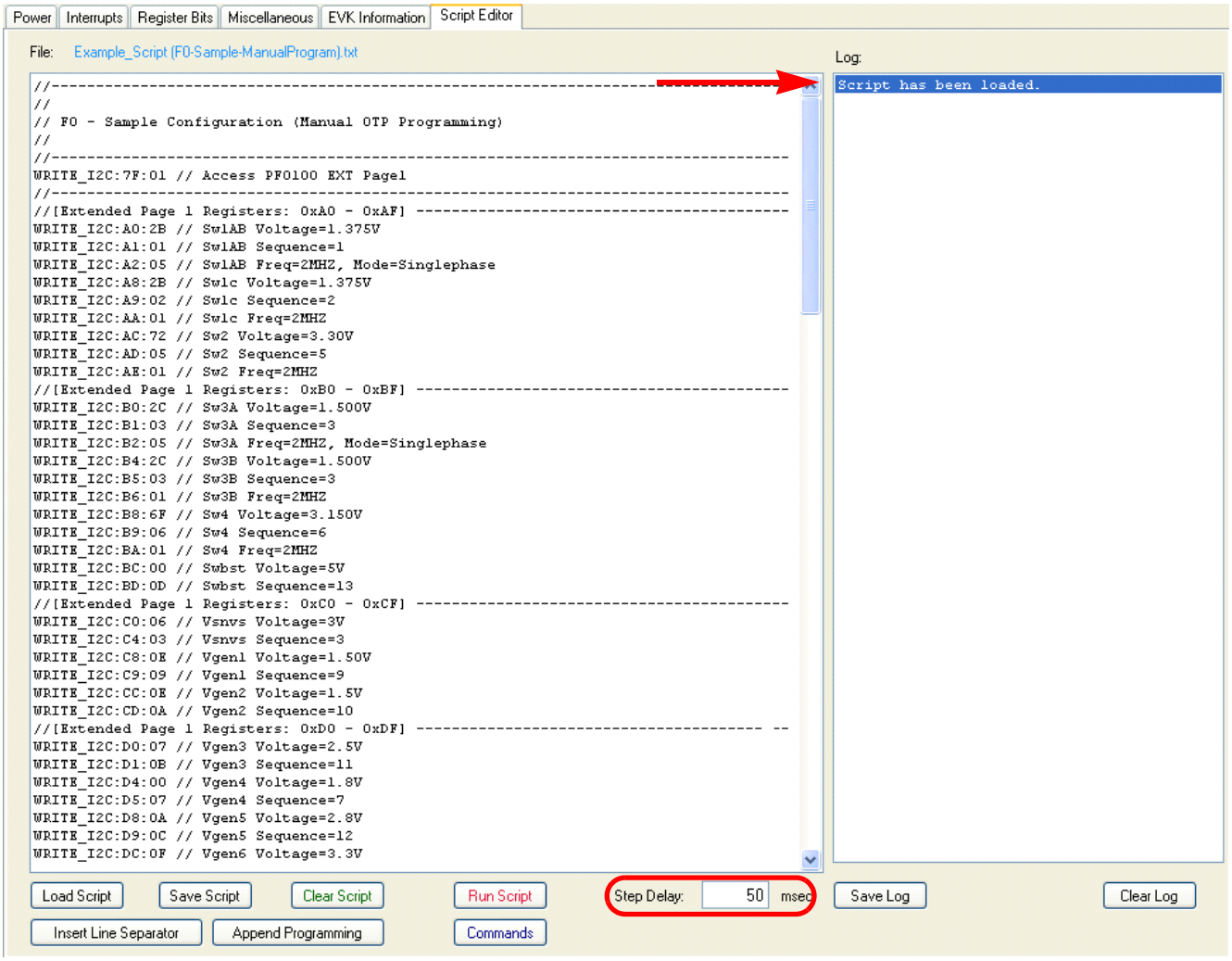


Figure 37. Script Dialog Box

Press the “Run Script” button to execute the script. As the script executes, each command will appear sequentially in the Script Log. Comments are ignored. When the script has completed, an entry in the Script Log will be made as shown in Figure 38.

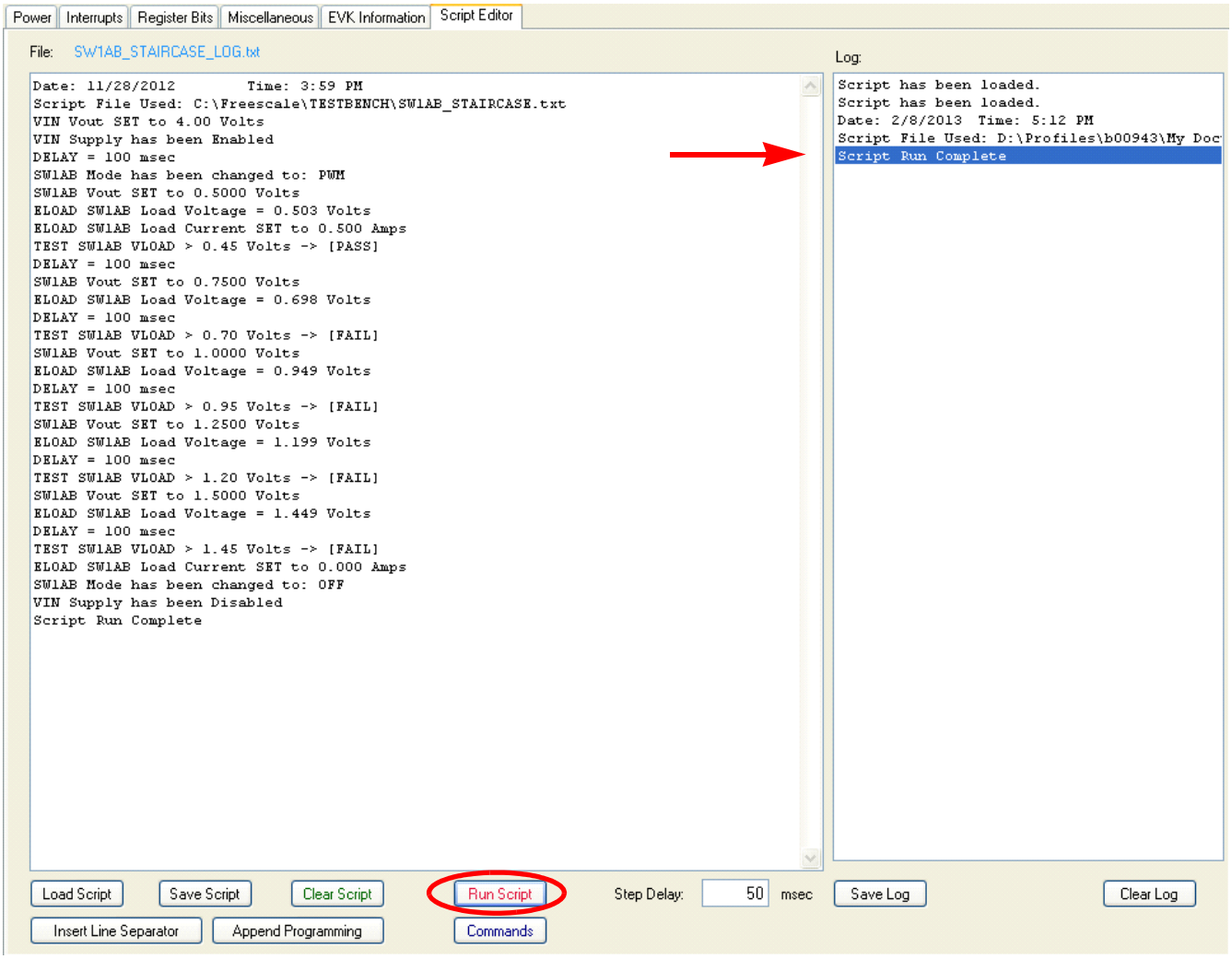


Figure 38. Running the Script

10.4.2 Writing a New Script

To write your own scripts, begin by creating a comment header using the “Insert Line Separator” button.

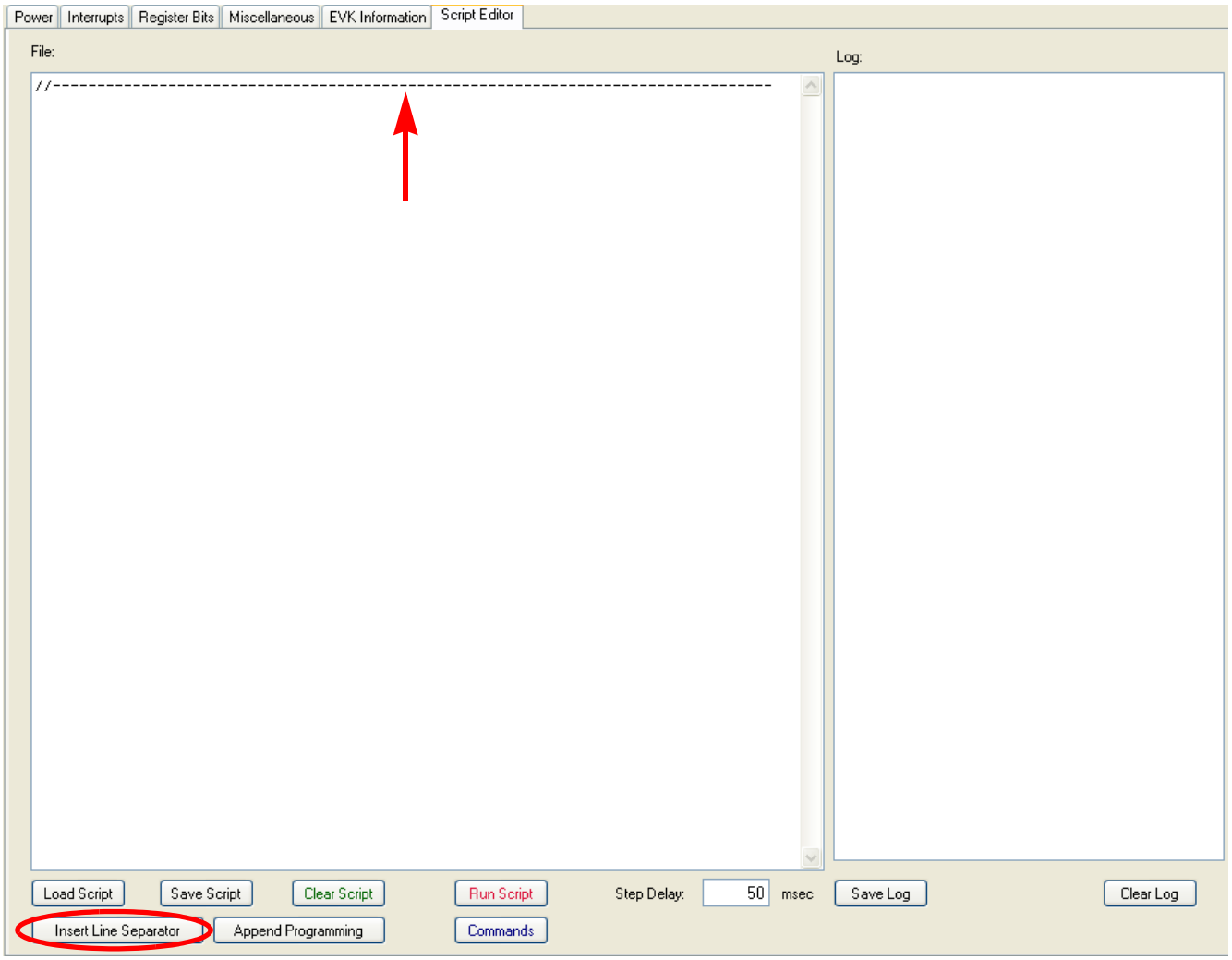


Figure 39. Inserting Line Separators

Proceed by manually writing the desired commands or use the “Command” button to display a graphical command selector in a new window, as shown in Figure 40.

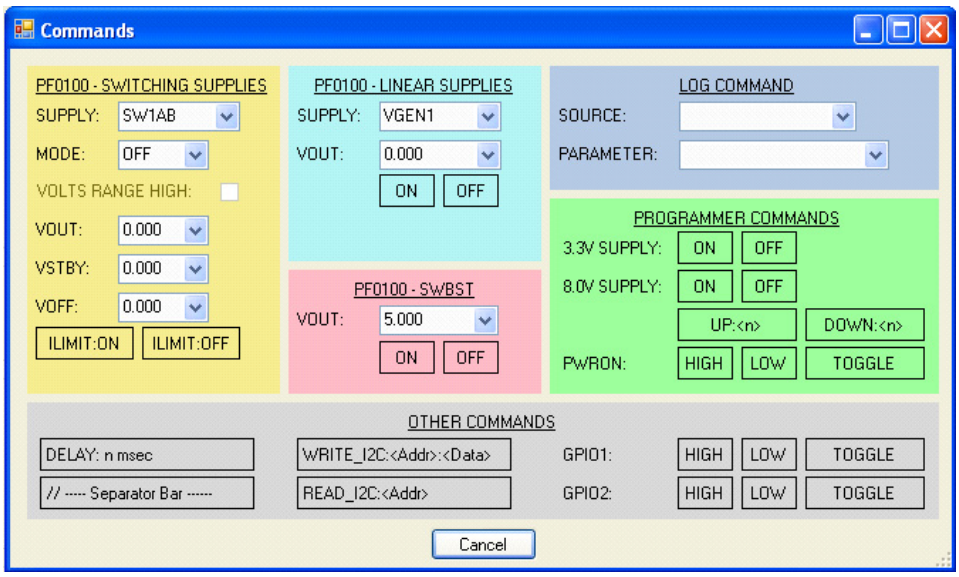


Figure 40. Command Selector Window

The “Command” window contains a set of commands that are useful for automatically sequencing the PF0100 power supplies, thereby emulating system behavior. The “Command” window is organized in six sections, as described below:

- PF0100 - SWITCHING SUPPLIES> place a single script command with the selected buck regulator and the desired function. The available functions are: mode selection, operating voltage setpoint, standby voltage setpoint, OFF voltage setpoint, enable current limit and disable current limit. Note that for SW2, SW3A/B and SW4, the VOLTS RANGE HIGH box need to be checked if the initial power up voltage is set to the high voltage operating range. If working in the lower voltage range, leave the box unchecked.
- PF0100 - LINEAR SUPPLIES> places a single script command with the selected LDO regulator and the desired function. The available functions are: operating voltage setpoint, enable and disable output.
- PF0100 - SWBST> Permits changing the operating voltage, as well as enabling and disabling the SWBST output.
- PROGRAMMER COMMANDS> Enables or disables the 3.3V supply as well as the ~8.0V boost supply on the KITPF0100EPEVBE. Allows a progressive step-up/step-down of the ~8.0V output and controls the general purpose output to set the PWRON terminal on the PF0100 high or set the same PWRON terminal low or toggle a pulse that triggers a PWRON event.
- OTHER COMMANDS> This section provides access to common instructions initiated by the control MCU. The possible commands include delay, add separator bar, generic I^2C write/read, set GPIO1 and GPIO2 high, low or toggle.
- LOG COMMAND> provide a log report of the actual status of a specific configuration on the PMIC. Syntax for the log commands are shown in Table 8.

10.4.2.1 Syntax and Command Set

Delimiters

- ':' - Is used as a separator
- '/' - Anything after a '/' will be ignored.
- White spaces will be truncated.

Table 8. Command List[(2)]

Command	Description
WRITE_I2C:<Addr>:<Data>	Sends <Data> to I^2C register <Addr>.[(3)]
READ_I2C:<Addr>	Reads the value of <Addr> and displays it in the Script Log. [(3)]
VPGM:ON	Enables the 8.0 V OTP programming supply.
VPGM:OFF	Disables the 8.0 V OTP programming supply.
VPGM:UP:<n>	Increases the OTP programming voltage (VPGM) in <n> DAC steps.
VPGM:DOWN:<n>	Decreases the OTP programming voltage (VPGM) in <n> DAC steps.
V3V3:ON	Enables the 3.3 V system supply.
V3V3:OFF	Disables the 3.3 V system supply.
PWRON:HIGH	Releases the PWRON signal to a high-impedance state, allowing the PF0100 to start up.
PWRON:LOW	Asserts the PWRON signal LOW, forcing the PF0100 to shutdown.
PWRON:TOGGLE	Asserts the PWRON signal LOW, and then releases it to a high-impedance state, generating a power on event on the PF0100.
DELAY:<value>	Adds delay between script commands. Note that delays are cumulative with the Script Delay set on the Editor. delay is set in ms.
GPIO1:HIGH	Releases the GPIO1 signal to a high-impedance state.
GPIO1:LOW	Asserts the GPIO1 signal LOW.
GPIO1:TOGGLE	Asserts the GPIO1 signal LOW, and then releases it to a high-impedance state.
GPIO2:HIGH	Releases the GPIO2 signal to a high-impedance state.
GPIO2:LOW	Asserts the GPIO2 signal LOW.
GPIO2:TOGGLE	Asserts the GPIO2 signal LOW, and then releases it to a high-impedance state.
SW1x:MODE:<operator>	Sets the mode of operation of the SW1x regulator. The valid operators are as follows: • OFF • PFM • PWM • APS
SW1x:VOUT:<value>	Sets the SW1x output voltage in normal operation. Operating range from 0.300 V to 1.875 V in 0.025 V steps.

Table 8. Command List[2]

Command	Description
SW1x:VSTBY:<value>	Sets the SW1x output voltage to the STANDBY mode. Operating range from 0.300 V to 1.875 V in 0.025 V steps.
SW1x:OFF:<value>	Sets the SW1x output voltage to the OFF Mode. Operating range from 0.300 V to 1.875 V in 0.025 V steps.
SW1x:ILIM:<operator>	Enables/disables the SW1x current limit. Valid operators: • ON • OFF
SWx:MODE:<operator>	Sets the mode of operation of the SWx regulator. Following are valid operators: • OFF • PFM • PWM • APS
SWx:VOUT:<value>	Sets the SWx output voltage to normal operation. Full operating range from 0.300 V to 3.300 V divided into two operating ranges[4]: • Low Voltage Range > 0.300 V to 1.875 V in 0.025 V steps. • High voltage Range > 0.800 V to 3.300 V in 0.050 V steps.
SWx:VSTBY:<value>	Sets the SWx output voltage to the STANDBY mode. Full operating range from 0.300 V to 3.300 V divided in two operating ranges[4]: • Low Voltage Range > 0.300 V to 1.875 V in 0.025 V steps. • High voltage Range > 0.800 V to 3.300 V in 0.050 V steps.
SWx:OFF:<value>	Sets the SWx output voltage to the OFF mode. Full operating range from 0.300 V to 3.300 V divided into two operating ranges[4]: • Low Voltage Range > 0.300 V to 1.875 V in 0.025 V steps. • High voltage Range > 0.800 V to 3.300 V in 0.050 V steps.
SWx:ILIM:<operator>	Enables/disables the SWx current limit. Valid operators: • ON • OFF
SWBST:VOUT:<value>	Set the output voltage of the SWBST regulator. Valid output voltage: • 5.000 • 5.050 • 5.100 • 5.150
SWBST:ON	Enables SWBST regulator
SWBST:OFF	Disables SWBST regulator.
VGENx:ON	Enables the VGENx supply.
VGENx:OFF	Disables the VGENx supply.
VGENx:VOUT:<value>	Sets the output voltage for VGENx supply. • VGEN1/2 operating range: 0.800 V to 1.550 V with 50 mV steps. • VGEN3/4/5/6 operating range: 1.800 V to 3.3 V with 100 mV steps.
VREFDDR:ON	Enables the VREFDDR supply.

Table 8. Command List(2)

Command	Description
VREFDDR:OFF	Disables the VREFDDR supply.
VSNVS:ON	Enables the VSNVS supply
VSNVS:OFF	Disables the VSNVS supply.
PWRON:Float	Releases the PWRON signal to a high-impedance state, allowing the PF0100 to start up. (Legacy for Revision A scripts)
LOG Commands	
LOG:SWx:<log operator>	Shows the current value of the <log operator> for the SWx regulator. Log operators: • VOUT = Output voltage in normal operation. • STBY = Output voltage in STANDBY mode. • OFF = Output voltage in OFF mode. • MODE = Current switching mode set. • OTP_VOUT = Default power up voltage set through OTP. • OTP_SEQUENCE = Default power up sequence of regulator.
LOG:VGENx:<log operator>	Shows the current value of the <log operator> for the VGENx regulator. Log operators: • VOUT = Output voltage. • ENABLE = supply is ENABLED/DISABLED. • OTP_VOUT = Default power up voltage set through OTP. • OTP_SEQUENCE = Default power up sequence of regulator.
LOG:VSWBST:<log operator>	Shows the current value of the <log operator> for the VSWBST regulator. Log operators: • VOUT = Output voltage. • ENABLE = Supply is ENABLED/DISABLED. • OTP_VOUT = Default power up voltage set through OTP. • OTP_SEQUENCE = Default power up sequence of regulator.
LOG:VREFDDR:<log operator>	Shows the current value of the <log operator> for the VREFDDR regulator. Log operators: • ENABLE = supply is ENABLED/DISABLED. • OTP_SEQUENCE = Default power up sequence of regulator.
LOG:VSNVS:<log operator>	Shows the current value of the <log operator> for the VSNVS regulator. Log operators: • VOUT = Output voltage. • OTP_VOUT = Default power up voltage set through OTP.
LOG:OTP_PU_CONFIG:<log operator>	Shows the current value set as default by OTP. • SEQ_CLK_SPEED = programmed power up sequencing speed. • DVS_CLK_SPEED = programmed DVS speed. • PWRON_MODE = programmed PWRON pin active level. • PGOOD_ENABLE = Power good mode is on/off.

Table 8. Command List(2)

Command	Description
LOG:INT:<Int operator>	Shows the status of the corresponding interrupt bit. Interrupt operators are as follows: • 110_DEGREES • 120_DEGREES • 125_DEGREES • 130_DEGREES • SW1A_OVERCURRENT • SW1C_OVERCURRENT • SW2_OVERCURRENT • SW3A_OVERCURRENT • SW3B_OVERCURRENT • SW4_OVERCURRENT • SWBST_OVERCURRENT • VGEN1_OVERCURRENT • VGEN2_OVERCURRENT • VGEN3_OVERCURRENT • VGEN4_OVERCURRENT • VGEN5_OVERCURRENT • VGEN6_OVERCURRENT

2. All characters (except for the "Float" subcommand) have to be entered in uppercase.
3. The register and data values should be entered as hexadecimal numbers, for example: 0x20 is entered as 20.
4. The output voltage operating range is set during OTP programming and cannot be changed under normal PMIC control.

Figure 41 shows a small sample script which enables the VGEN1 supply and reads the SW1AB mode register. Run this script by pressing the “Run Script” Button. Note that the result for the READ_I2C:23 command shows up in the Script Log as 0x08.

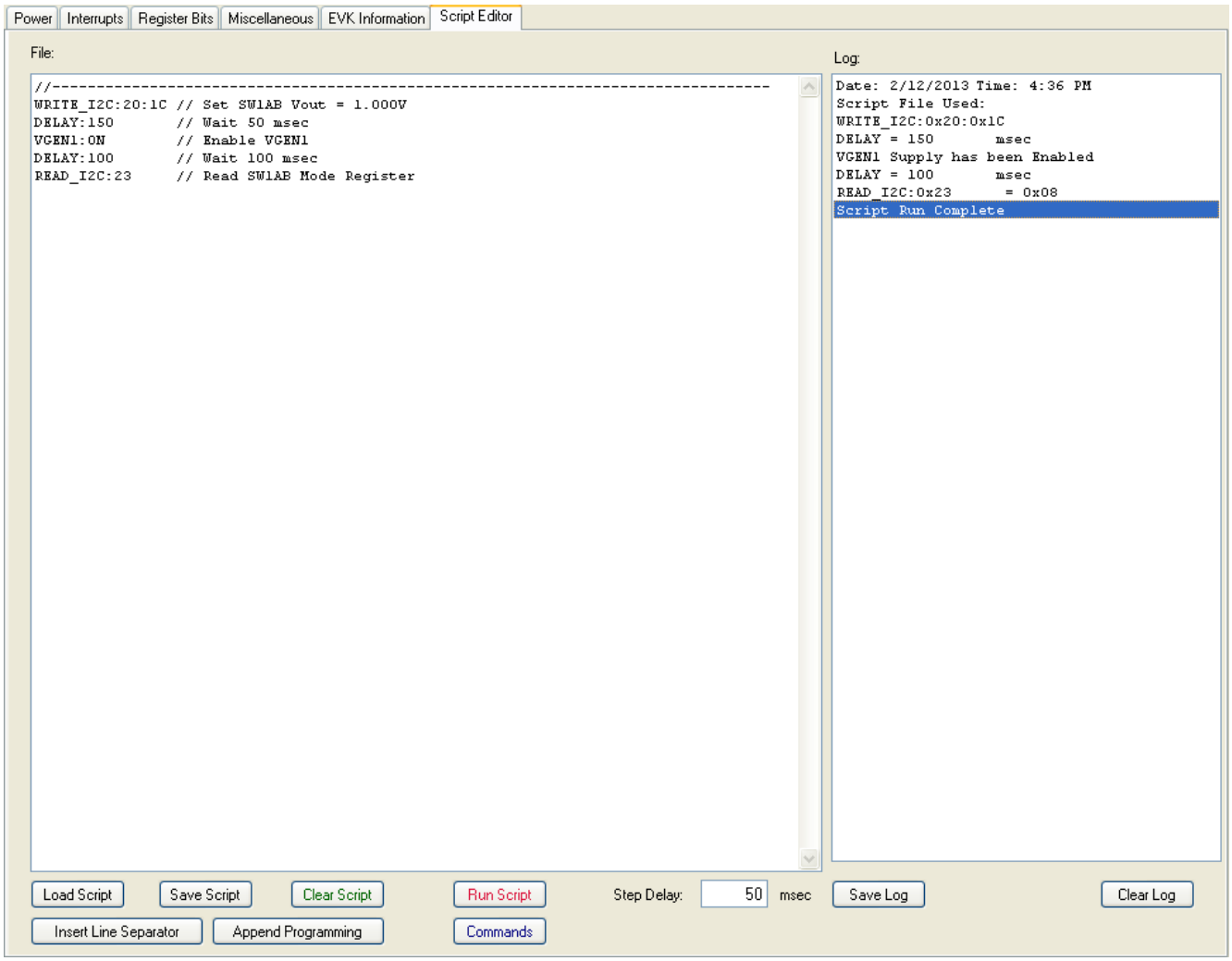


Figure 41. Sample Script

Confirm that the script has run correctly by checking the expected results in the GUI registers for the respective supplies.

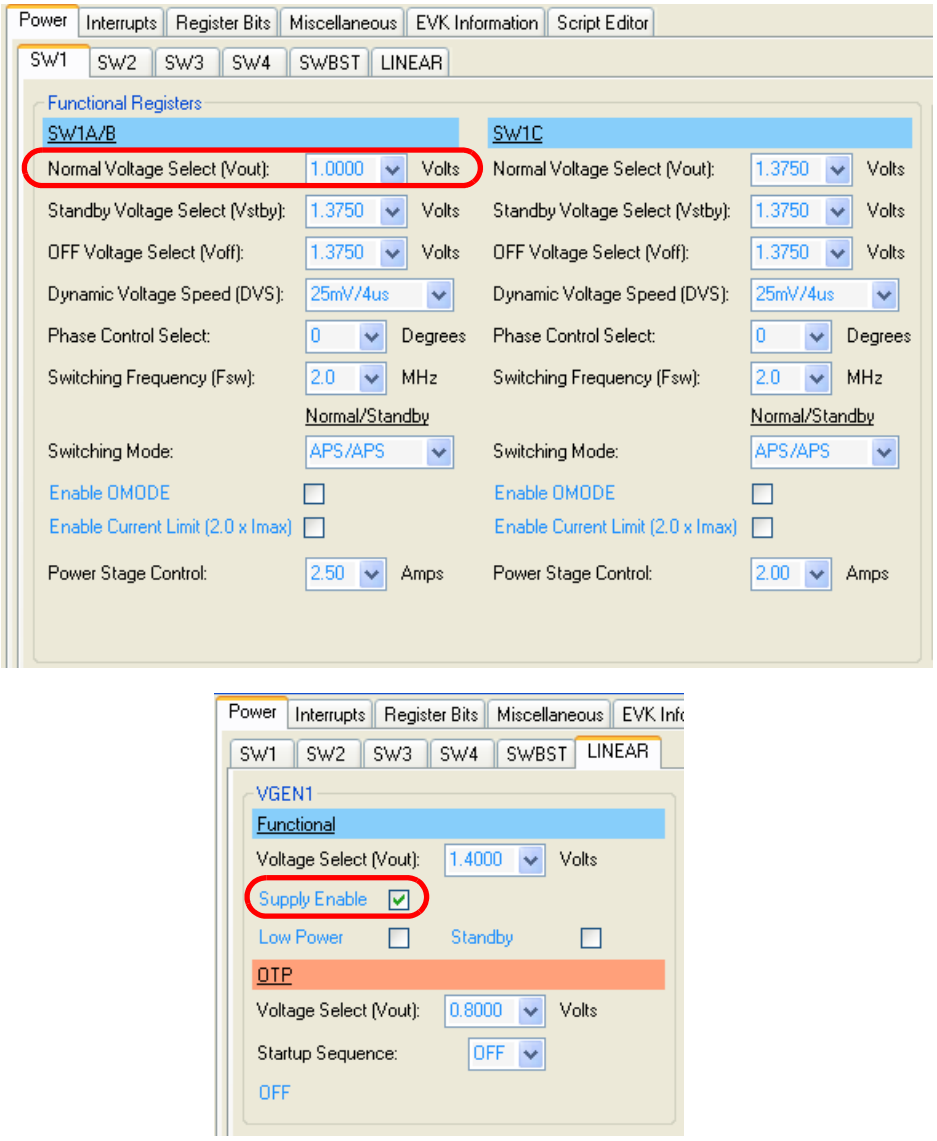


Figure 42. Verifying Script Results.

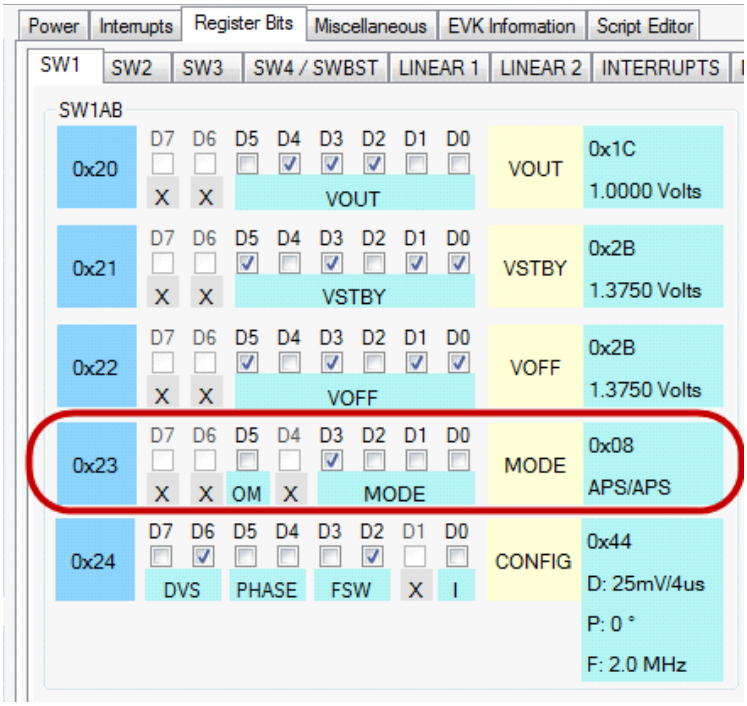


Figure 43. Verifying SW1 Mode Read Command

Note that the 0x08 SW1AB mode value in the Script Log (**Figure 41**) correlates with that in the register bits, as shown directly above.

Finally, save the script so that it can be used again. Press the “Save Script” button, then the “Save File” dialog box will appear. Enter the desired script file name, including the “.txt” file extension, then press the “Save” button.

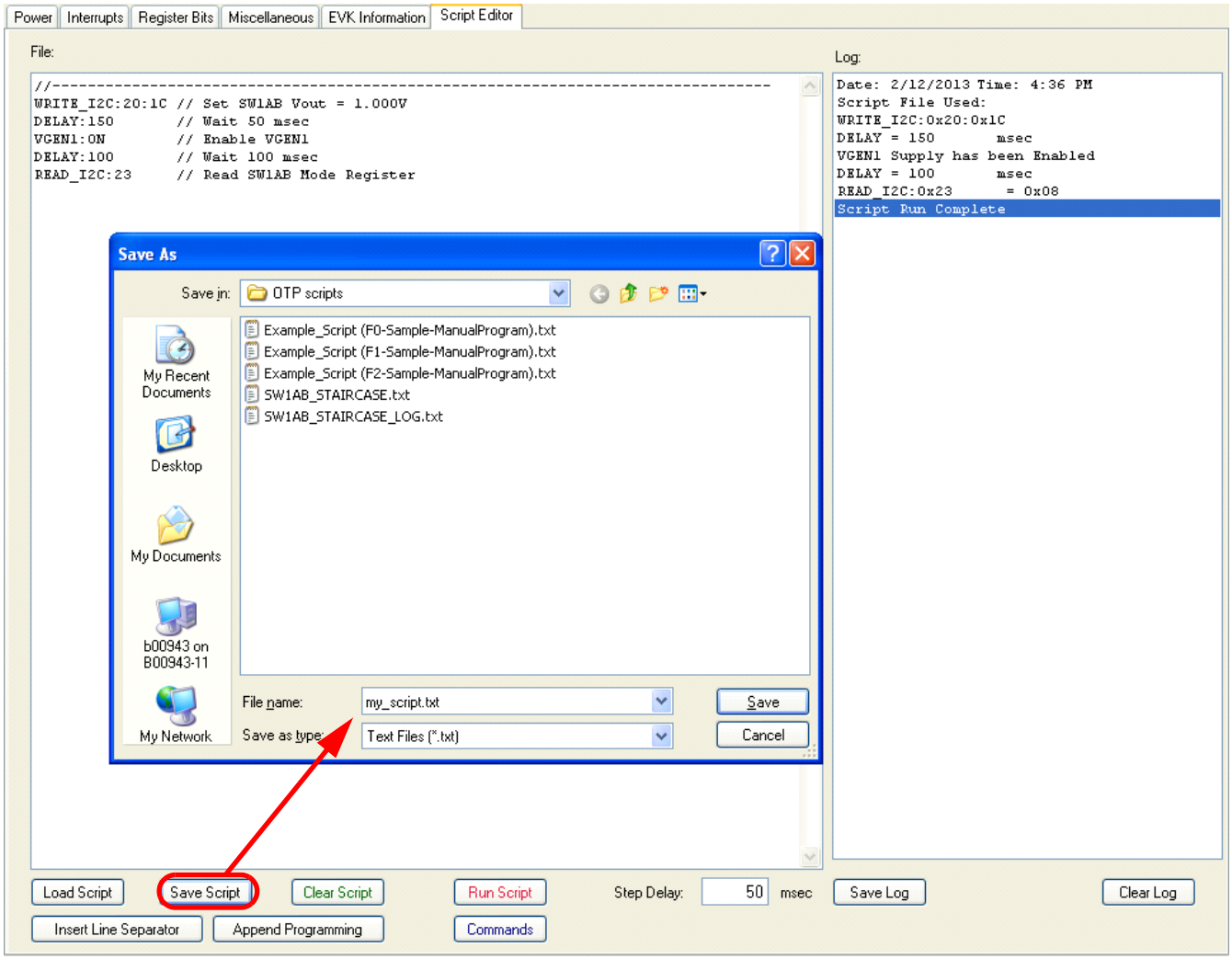


Figure 44. Saving a Script

10.5 Loading a Configuration File

A configuration file is a .txt file which contains specific OTP configuration instructions ready to be loaded and programmed into the OTP memory, thereby setting up a definitive power-up configuration for the PMIC. To load a configuration script file, press the “Load Configuration” button. An “Open File” dialog box will appear so that you can browse for and select your desired script file. Once you have selected the file you want, press the “Open” button.

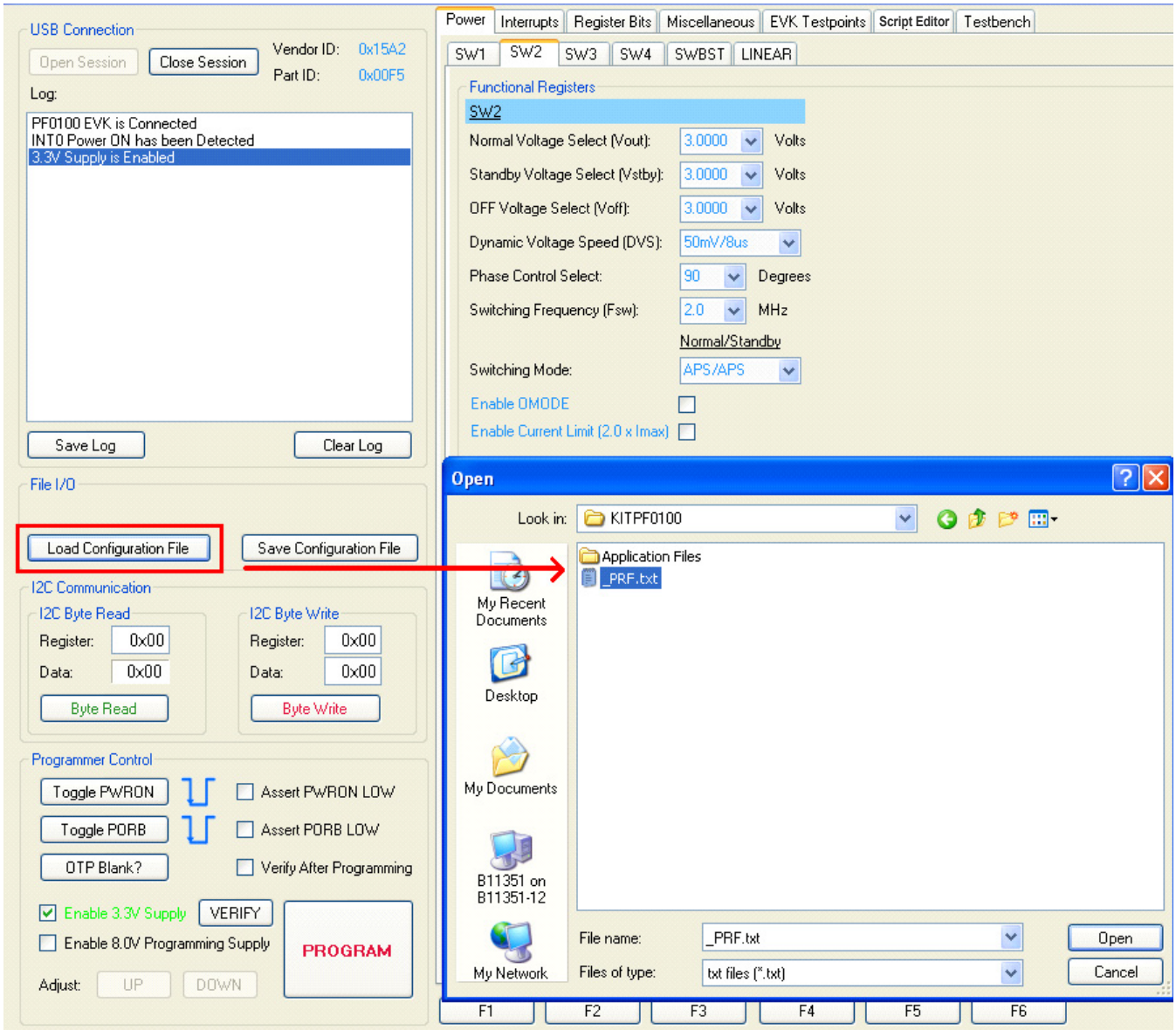


Figure 45. Loading a Configuration File

When the file has loaded, an entry in the Log List will be made, and you should see the selected file displayed in the File I/O box.

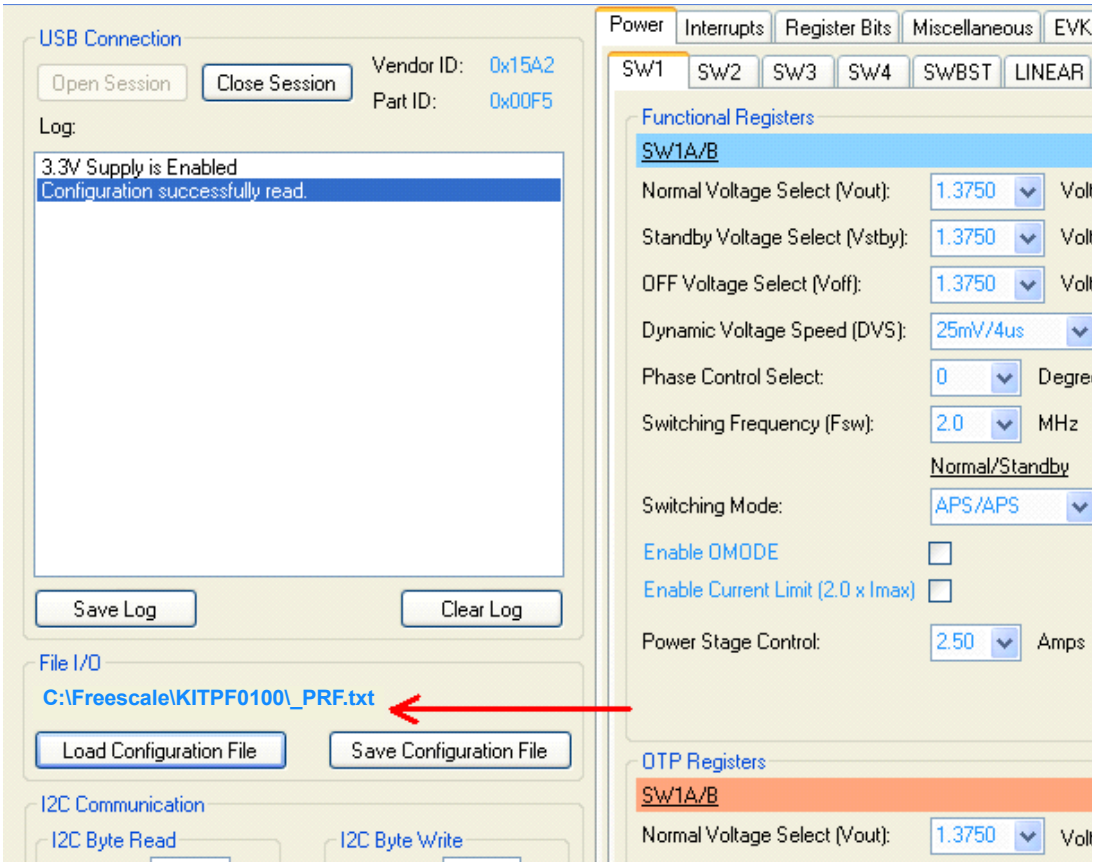


Figure 46. Scripting Tab

The “Save Configuration” button can be used to extract the current values of the PF0100 OTP Extended Page 1 registers from 0xA0 to 0xFF and place them in a text file, creating a mirror image of the OTP configuration of the PMIC in use. Remember to add the .txt file extension.

10.6 Programming an External PF0100 Through J36

If the KITPF0100EPEVBE is used as an external programmer for either a customer board or a dedicated PF0100 programming socket, J36 provides the required signals for such a task, however, it will be necessary to isolate the communication signals from the on-board PMIC by doing the following:

1. Verify that J22 is NOT in position 1-2
2. Verify that J17 is NOT in position 1-2
3. Verify that J30 is NOT in position 1-2
4. Remove R43 (bottom layer)
5. Remove R46 (bottom layer)
6. Remove R47 (bottom layer)

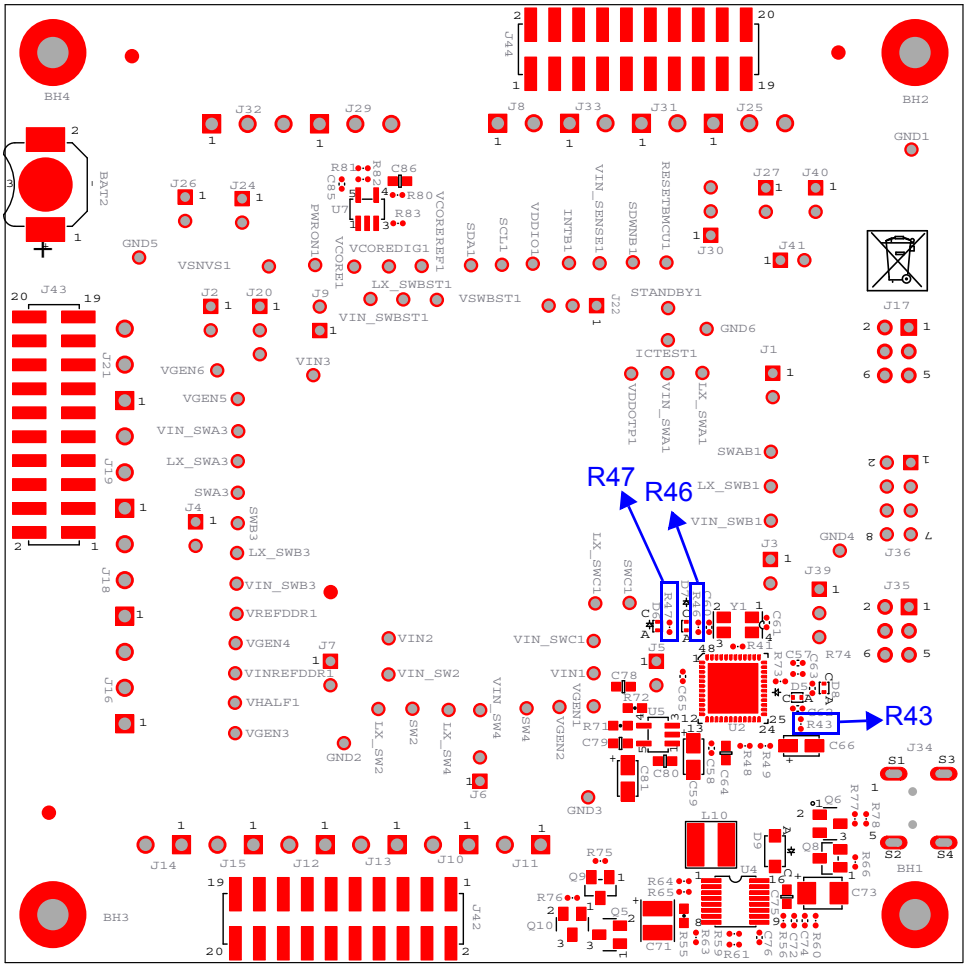


Figure 47. KITPF0100EPEVBE Bottom View - Components Location

At this point it might be a good idea to check if the PF0100 part to be programmed is blank (not programmed). This can be easily done by pressing the “OTP Blank?” button.

If you would like the KITPF0100GUI to verify that a part has been programmed with the OTP data supplied by the programming script, click the “Verify After Programming” check box. This will direct the GUI to do a line-by-line comparison between the data written and the data actually programmed into the part.

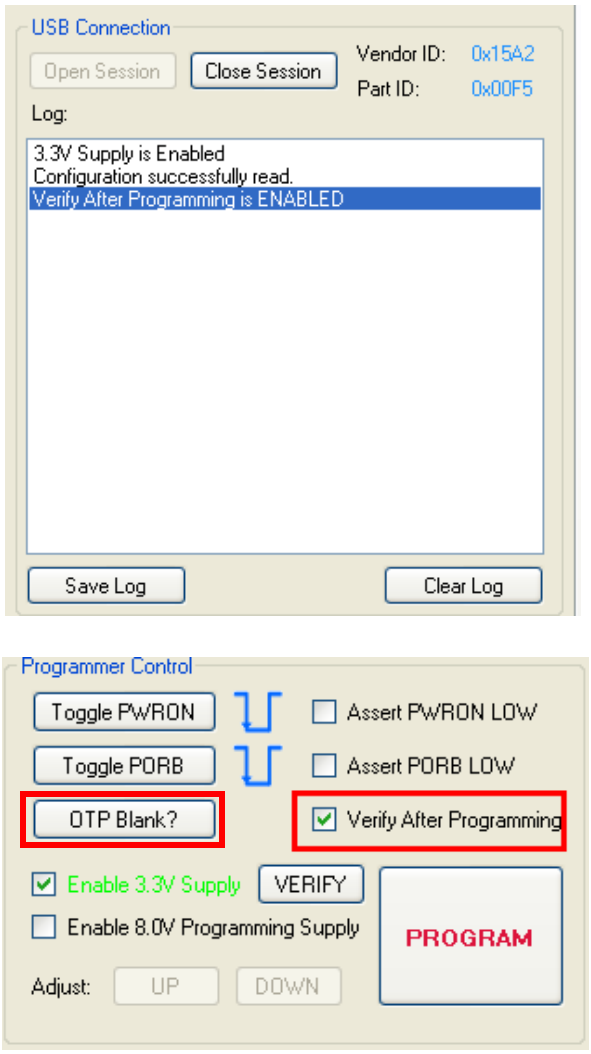


Figure 48. Verify After Programming and OTP Blank?

Then press the “PROGRAM” button. The KITPF0100GUI will verify that the script file has been loaded and the supply voltages have been applied before starting the programming sequence. Each step of the programming sequence will be displayed in the Log List.

When the programming sequence turns on the 8.0V VPGM programming supply, then the red LED D11 of the KITPF0100EPEVBE will be on.

After programming has been completed, the GUI will automatically check to see if the OTP memory has been programmed, and because we selected “Verify” afterwards, the verify algorithm will be run. The number of OTP programming errors will be reported in the Log List.

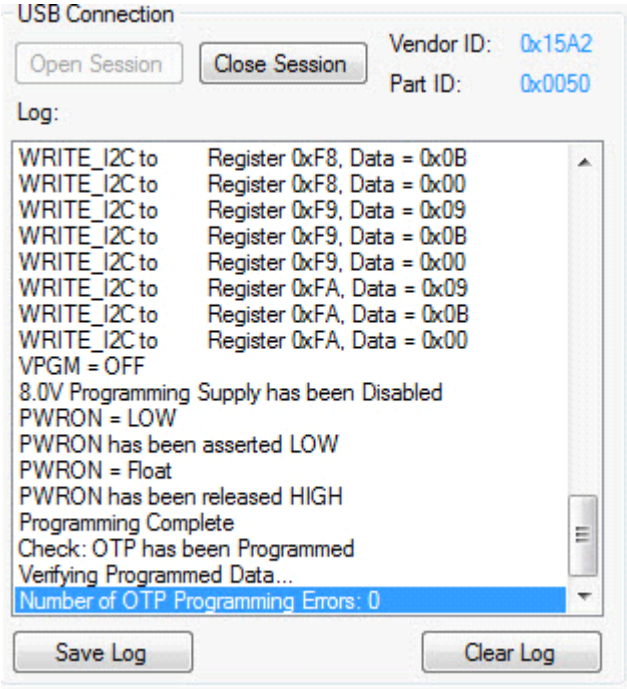


Figure 49. Scripting Log Session Example

Note: If it is desired to carry out One-Time Programming of the PF0100 device soldered on the KITPF0100EPEVBE evaluation board, ensure that the board hardware is correctly configured according to the chosen OTP settings.

Furthermore, the KITPF0100EPEVBE allows the configuration of the SW2 regulator or an external 3.3V LDO output as the VDDIO/I^2C pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J30 = 3-2). If the SW2 regulator is to be set below 3.0V then make sure the 3.3V LDO output is connected to VDDIO and the I^2C pull-up resistors by removing R34 and R33 and shorting pins 1, 2 and 3 of J30.

11 KITPF0100EPEVBE Board Layout

11.1 Assembly Layer Top

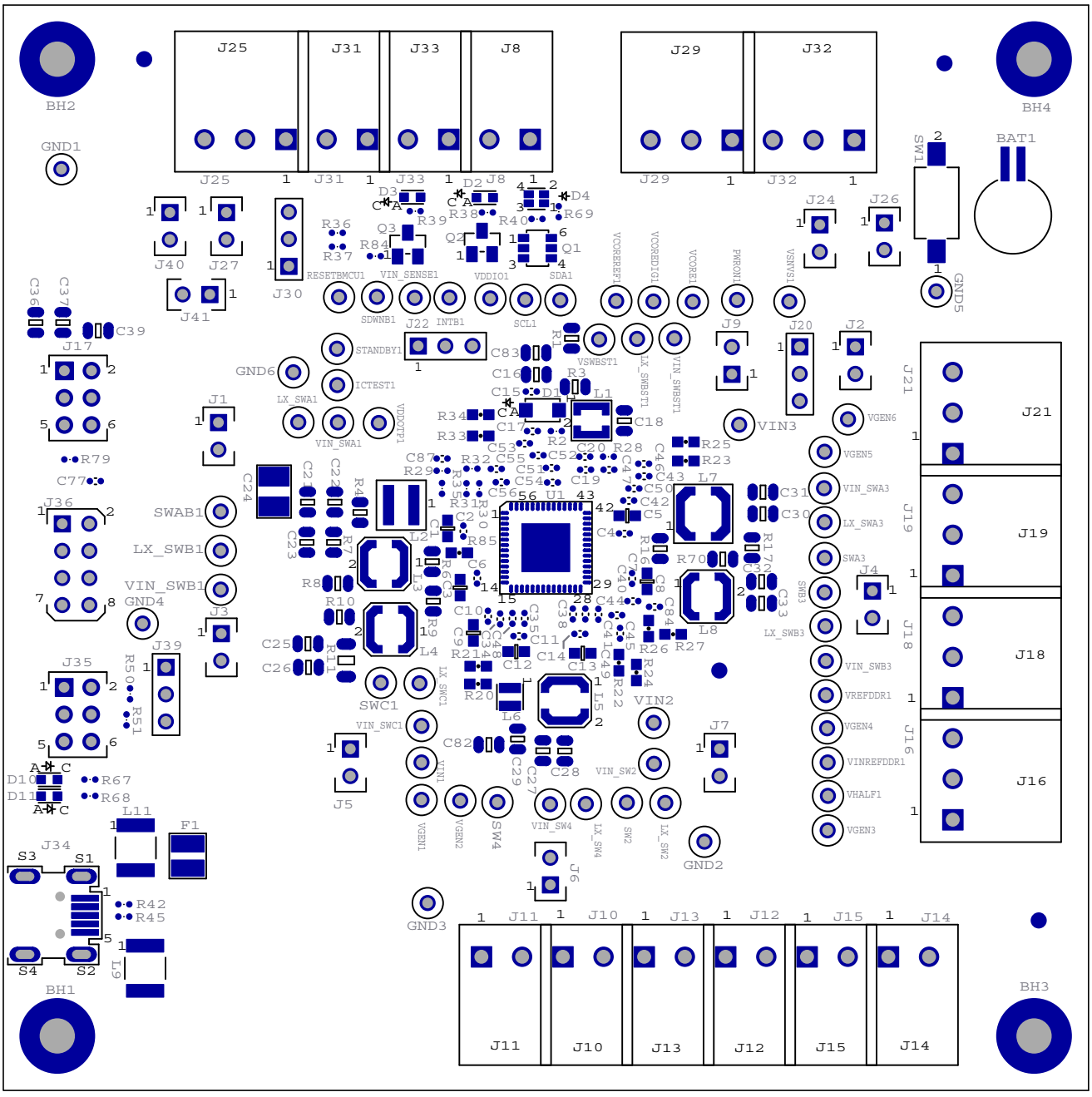


Figure 50. Assembly Top Layer

11.2 Assembly Layer Bottom

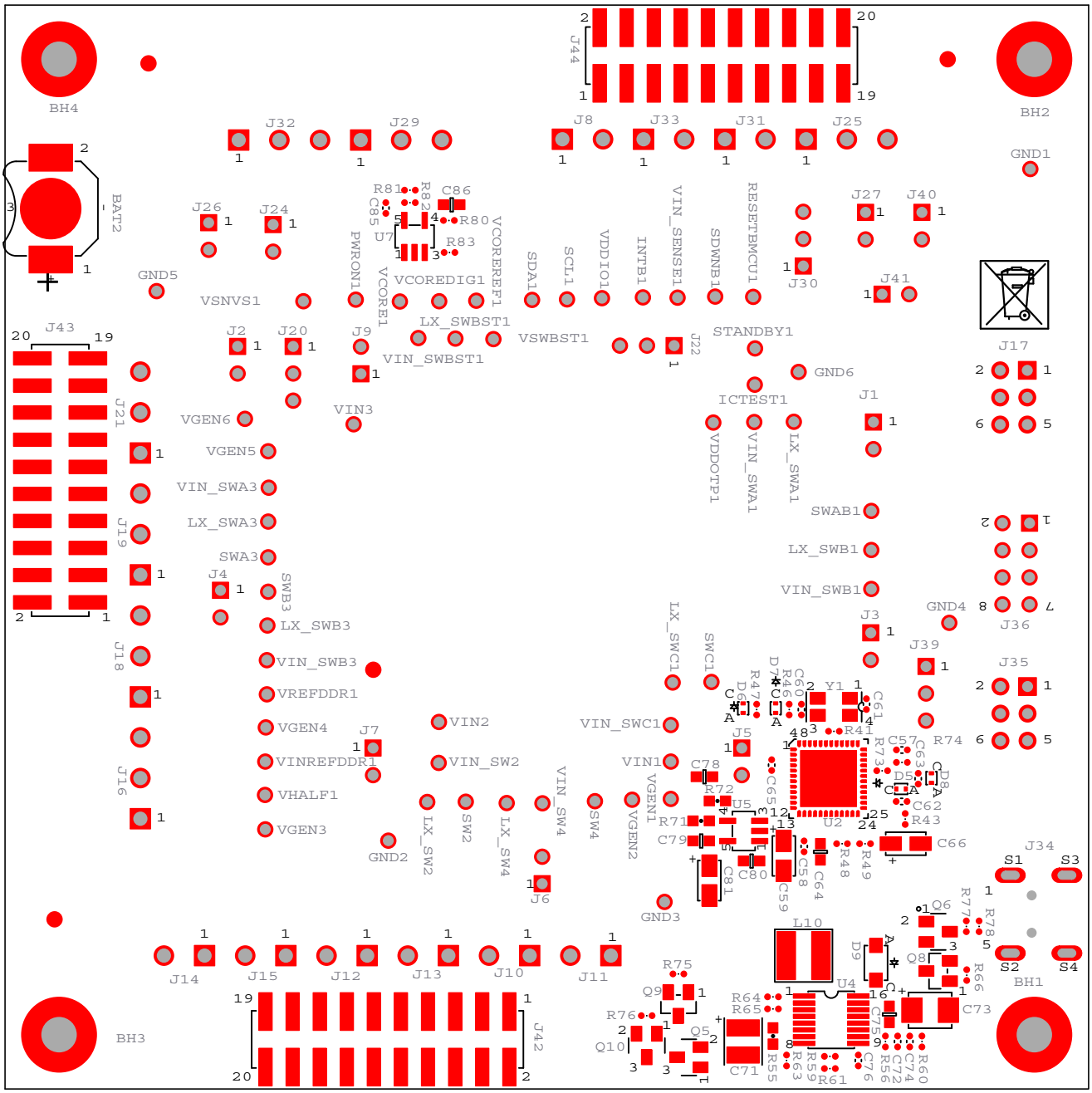


Figure 51. Assembly Layer Bottom

11.3 Top Layer Routing

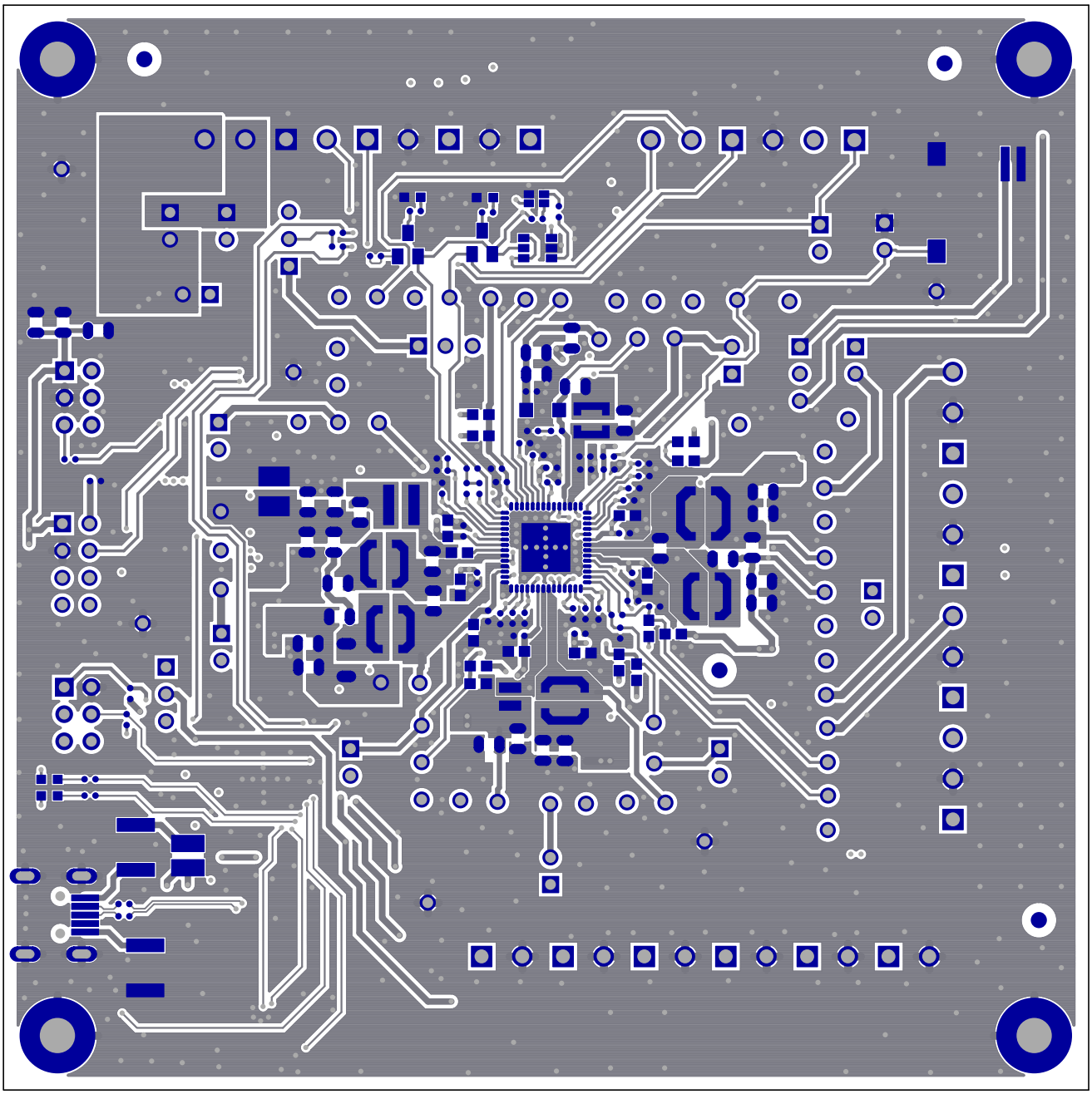


Figure 52. Top Layer Routing

11.4 Inner Layer 1 Routing

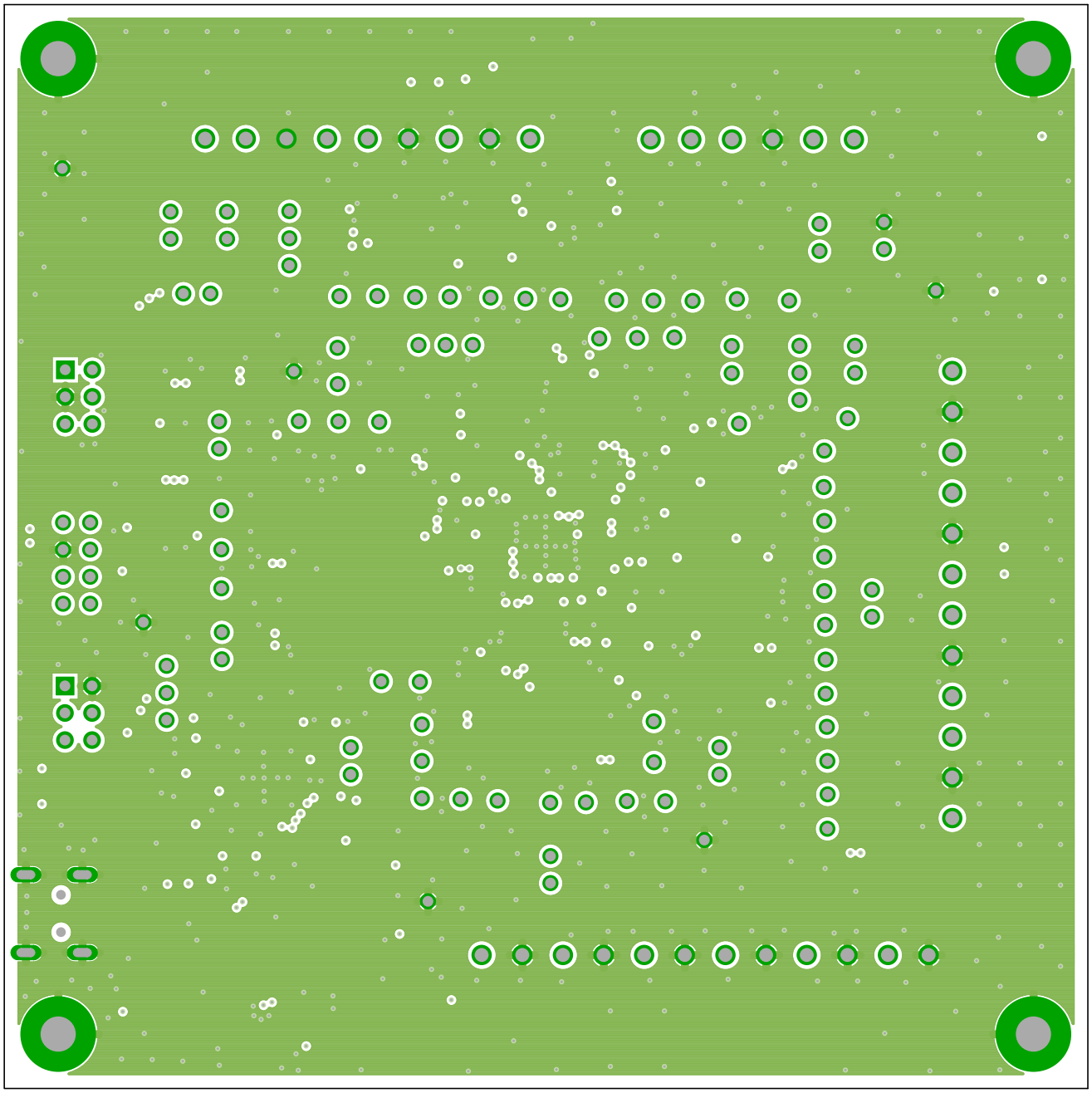


Figure 53. Inner Layer 1 Routing

11.5 Inner Layer 2 Routing

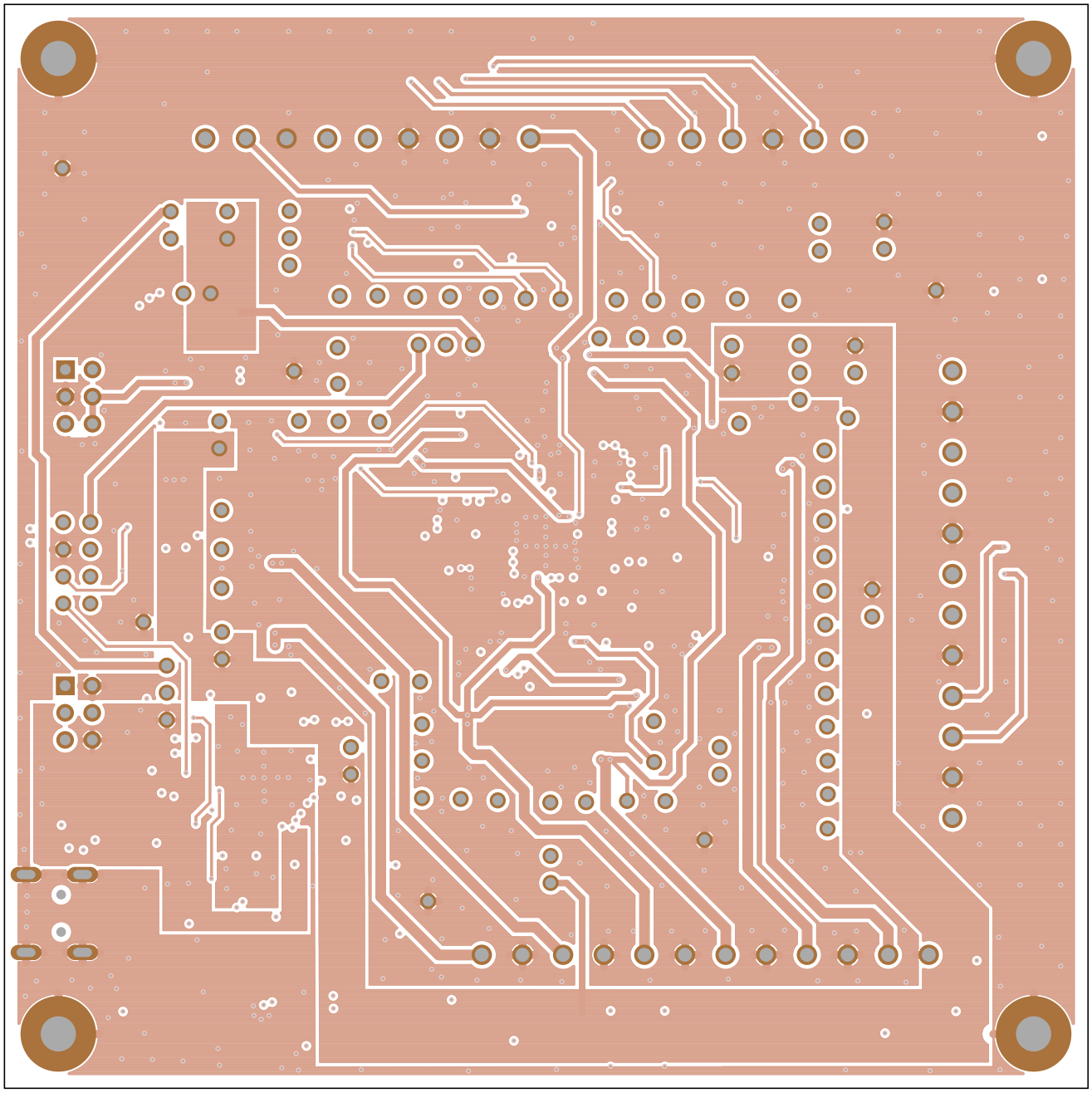


Figure 54. Inner Layer 2 Routing

11.6 Bottom Layer Routing

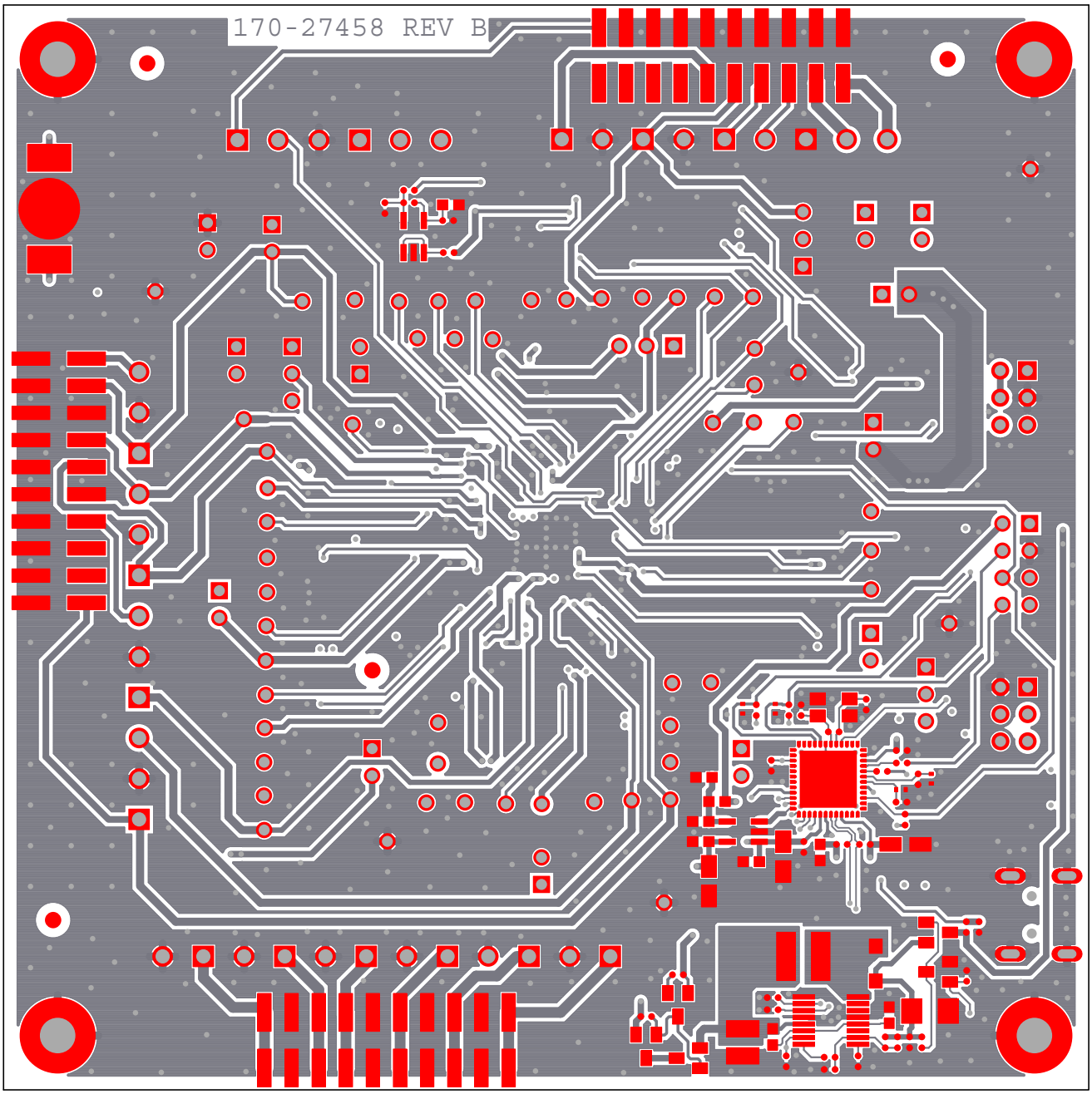


Figure 55. Bottom Layer Routing

12 Bill of Materials

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
1	1		BAT1	BATTERY LITHIUM -- 3V 5.5MAH	MS621F-FL11E	SII MICRO PARTS LTD.
2	1		BAT2	HOLDER COIN CELL 6.8MM SMT	BK-879	MEMORY PROTECTION DEVICES INC
3	4		BH1, BH2, BH3, BH4	MOUNTING HOLE 0.130 INCH, NOT A PART TO ORDERr	NOT A PART TO ORDER	NO MFG
4	7		C1, C3, C5, C8, C9, C12, C13	CAP CER 4.7µF 10V 10% X5R 0603		
5	7		C2, C6, C10, C11, C14, C44, C45	CAP CER 0.1µF 10V 10% X5R 0402		
6	5		C4, C7, C19, C56, C77	CAP CER 0.1µF 10V 10% X7R 0402		
7	1		C15	CAP CER 0.01µF 50V 10% X7R 0402		
8	14		C16, C21, C22, C25, C26, C27, C28, C29, C30, C31, C32, C33, C82, C83	CAP CER 22µF 10V 20% X5R 0805		
9	1	DNP	C17	CAP CER 1000PF 50V X7R 5% 0402		
10	1		C18	CAP CER 10µF 10V 10% X7R 0805		
11	5		C20, C34, C38, C42, C43	CAP CER 2.2µF 6.3V 20% X5R 0402		
12	1	DNP	C23	CAP CER 22µF 10V 20% X5R 0805		
13	1	DNP	C24	CAP CER 22µF 10V 10% X7R 1210		
14	2		C35, C41	CAP CER 4.7µF 6.3V 20% X5R 0402		
15	3		C36, C37, C39	CAP CER 10µF 16V 10% X7R 0805		

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
16	9		C40, C48, C49, C50, C51, C52, C54, C84, C87	CAP CER 1.0µF 10V 10% X5R 0402		
17	2		C46, C53	CAP CER 0.22µF 16V 10% X7R 0402		
18	1		C47	CAP CER 0.47µF 10V 10% X7R 0402		
19	1	DNP	C55	CAP CER 1.0µF 10V 10% X5R 0402		
20	5		C57, C58, C62, C63, C65	CAP CER 0.1µF 16V 10% X5R 0402		
21	1		C59	CAP TANT 10µF 16V 10% -- 3216-18		
22	3		C60, C61, C72	CAP CER 22PF 25V 5% C0G 0402		
23	1		C64	CAP CER 0.47µF 16V 10% X7R 0603		
24	1		C66	CAP TANT 4.7µF 10V 10% -- 3216-18		
25	1		C71	CAP TANT ESR 0.600 OHMS 15µF 25V 10% -- 3528-21		
26	1		C73	CAP TANT 4.7µF 25V 10% -- 3528-21		
27	1		C74	CAP CER 0.1µF 25V 10% X5R 0402		
28	1		C75	CAP CER 1.0µF 25V 10% X5R 0603		
29	1		C76	CAP CER 0.1µF 6.3V 10% X7R 0402		
30	2		C78, C86	CAP CER 470PF 50V 5% COG 0603		
31	1	DNP	C79	CAP CER 2.2µF 16V 10% X5R 0603		
32	1		C80	CAP CER 1.0µF 16V 10% X5R 0603		
33	1		C81	CAP TANT ESR=1.800 OHMS 2.2µF 10V 10% 3216-18		
34	1	DNP	C85	CAP CER 2.2µF 6.3V 20% X5R 0402		

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
35	1		D1	DIODE SCH PWR RECT 1A 20V SMT	MBR120LSFT1G	ON SEMICONDUCTOR
36	3		D2, D3, D11	LED RED SGL 30MA 0603	SML-LXFM0603SIC-TR	LUMEX
37	1		D4	LED DUAL GRN/RED 30MA SMT	LTST-C195KGJRKT	LITE ON
38	4		D5, D6, D7, D8	DIODE TVS ESD PROT ULT LOW CAP 5-5.4V SOD-923	ESD9L5.0ST5G	ON SEMICONDUCTOR
39	1		D9	DIODE SCH PWR RECT 1A 30V SOD-123	MBR130LSFT1G	ON SEMICONDUCTOR
40	1		D10	LED GRN SGL 30MA SMT 0603	SML-LXFM0603SUGCTR	LUMEX
41	1		F1	FUSE PLYSW 0.5A 13.2V SMT	MICROSMD050F-2	RAYCHEM
42	56	DNP	-	TEST POINT RED 40 MIL DRILL 180 MIL TH 109L		
43	13		J1, J2, J3, J4, J5, J6, J7, J9, J24, J26, J27, J40, J41	HDR 1X2 TH 100MIL SP 339H AU 118L		
44	9		J8, J10, J11, J12, J13, J14, J15, J31, J33	SUBASSEMBLY CON 1X2 TB TH 3.81MM SP 201H -- 138L + TERM BLOCK PLUG 3.81MM 2POS		
45	7		J16, J18, J19, J21, J25, J29, J32	SUBASSEMBLY CON 1X3 TB TH 3.81MM SP 201H -- 138L + TERM BLOCK PLUG 3.81MM 3POS		
46	2		J17, J35	HDR 2X3 TH 100MIL CTR 335H AU 95L		
47	4		J20, J22, J30, J39	HDR 1X3 TH 100MIL SP 340H AU 118L		
48	1		J34	CON 5 USB MINI-B RA SHLD SKT SMT 31MIL SP AU	675031340	MOLEX
49	1		J36	HDR 2X4 TH 100MIL CTR 425H AU 310L		
50	3	DNP	J42, J43, J44	HDR 2X10 SMT 100MIL SP 383H AU		
51	1		L1	IND PWR 2.2UH@100KHZ 2.0A 20% SMT	LPS3015-222ML_	COILCRAFT
52	1		L2	IND PWR 1UH@100kHz 6A 20% SMT	XAL4020-102MEC	COILCRAFT

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
53	4		L3, L4, L5, L8	IND PWR 1UH@100KHZ 2.4A 30% SMT	LPS4012-102NLC	COILCRAFT
54	1		L6	IND PWR 1UH@1MHZ 2A 30% SMT	VLS252010T-1R0N	TDK
55	1		L7	IND PWR 1UH@100KHZ 2.65A 20% SMT	LPS5015-102MLC	COILCRAFT
56	1		L9	IND FER 100 OHM@100MHZ 8A 25% SMD/1812	HI1812V101R-10	LAIRD TECHNOLOGIES
57	1		L10	IND PWR CHK 22UH@1KHZ 1A 20% SMD	744773122	WURTH ELEKTRONIK EISOS GMBH & CO. KG
58	1		L11	IND FER 100 OHM@100MHZ 8A 25% SMD/1812	HI1812V101R-10	LAIRD TECHNOLOGIES
59	1		Q1	TRAN MOSFET DUAL N & P CHANNEL 2.5V S-SOT6	FDC6327C	FAIRCHILD
60	2		Q2, Q3	TRAN PMOS SW 120MA 25V SOT23	FDV302P	FAIRCHILD
61	3		Q5, Q6, Q10	TRAN PMOS SW 2A 30V SSOT3	FDN360P	FAIRCHILD
62	2		Q8, Q9	TRAN NMOS 50V 220MA SOT-23	BSS138	FAIRCHILD
63	6		R1, R3, R4, R6, R8, R16	RES -- 0.001 OHM 1/4W 5% 0805	LMI-R001-5.0	ISABELLENHÜTTE HEUSLER GMBH & CO. KG
64	1	DNP	R2	RES MF 1.0 OHM 1/16W 1% 0402		
65	5	DNP	R7, R9, R10, R17, R70	RES -- 0.001 OHM 1/4W 5% 0805	LMI-R001-5.0	ISABELLENHÜTTE HEUSLER GMBH & CO. KG
66	1		R11	RES MF 0.001 OHM 1W 1% 1206	CSNL1206FT1L00	STACKPOLE ELECTRONICS
67	5	DNP	R20, R23, R24, R27, R33	RES MF ZERO OHM 1/10W 1% 0603		
68	6		R21, R22, R25, R26, R34, R85	RES MF ZERO OHM 1/10W 1% 0603		
69	2		R28, R41	RES MF 1.0M 1/16W 1% 0402		
70	2		R29, R79	RES MF 100K 1/16W 5% 0402		

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
71	3		R30, R31, R32	RES MF 10.0K 1/16W 1% 0402		
72	6		R35, R43, R46, R47, R73, R74	RES MF ZERO OHM 1/10W -- 0402		
73	4		R36, R37, R50, R51	RES MF 4.70K 1/16W 1% 0402		
74	4		R38, R39, R40, R69	RES MF 200 OHM 1/10W 1% 0402		
75	2		R42, R45	RES MF 33.0 OHM 1/16W 1% 0402		
76	2	DNP	R48, R49	RES MF 1.5K 1/16W 5% 0402		
77	1		R55	RES MF 100 OHM 1/10W 1% 0603		
78	1		R56	RES MF 604K 1/16W 1% 0402		
79	1		R59	RES MF 374K 1/16W 1% 0402		
80	2		R60, R76	RES MF 470K 1/16W 1% 0402		
81	1		R61	RES MF 120K 1/16W 1% 0402		
82	3		R63, R64, R65	RES MF 10K 1/16W 5% 0402		
83	2		R66, R75	RES MF 47K 1/16W 1% 0402		
84	2		R67, R68	RES MF 470 OHM 1/16W 1% 0402		
85	1		R71	RES MF 20K 1/10W 5% 0603		
86	1		R72	RES MF 12.0K 1/10W 1% 0603		
87	2		R77, R78	RES MF 100K 1/16W 1% 0402		
88	1		R80	RES MF 27K 1/16W 5% 0402		
89	1		R81	RES MF 470K 1/16W 5% 0402		
90	3	DNP	R82, R83, R84	RES MF ZERO OHM 1/10W -- 0402		
91	1	DNP	SW1	SW SPST PB 12V 50MA SMT		

Item	Qty	Assy Opt	Schematic Label	Value/Description	Part Number	Manufacturer
92	1		U1	IC POWER MANAGEMENT CONSUMER/INDUSTRIAL QFN56	MMPF0100NPEP	FREESCALE SEMICONDUCTOR
93	1		U2	IC MCU 8BIT 48MHZ 60KB FLASH 2.7-5.5V QFN48	MC9S08JM60CGTE	FREESCALE SEMICONDUCTOR
94	1		U4	IC DAC CTRL BOOST INV +/-27.5V -- 2.7-5.5V QSOP16	MAX686EEE+	MAXIM
95	2		U5, U7	IC LIN VREG LDO 1.5-15V 150MA 2.5-16V SOT23-5	MIC5205YM5	MICREL
96	1		Y1	XTAL 12MHZ SER 9PF SMT	ECS-120-9-42X-CKM-TR	ECS INC. INTERNATIONAL

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application

13 References

Document Number	Description	URL
MMPF0100	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MMPF0100.pdf
MMPF0100ER	Errata	http://cache.freescale.com/files/analog/doc/errata/MMPF0100ER.pdf
PFSERIESFS	Fact Sheet	http://cache.freescale.com/files/analog/doc/fact_sheet/PFSeriesFS.pdf
AN4622	Layout Application Note	http://cache.freescale.com/files/analog/doc/app_note/AN4622.pdf
	Product Summary Page	www.freescale.com/MMPF0100
	Tool Summary Page	www.freescale.com/KITPF0100EPEVBE
	Analog Home Page	www.freescale.com/analog
	Power Management Home Page	www.freescale.com/PMIC

13.1 Support

Visit Freescale.com/support for a list of phone numbers within your region.

13.2 Warranty

Visit Freescale.com/warranty for a list of phone numbers within your region.

14 Revision History

Revision	Date	Description of Changes
1.0	11/2012	• Initial Release
2.0	2/2013	• Updated document for the latest GUI Revision 3.0.0.20 • Added Figure 14. to section **8 Evaluation Board Schematic** • Added TBB operation Mode. • Updated section **10.4 Using the Script Editor** • Updated section **10.5 Loading a Configuration File**

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: KTPF0100UG
Rev. 2.0
2/2013

freescale™